ZR-5800-II

SHARP SERVICE MANUAL

V16051

CODE: 00ZZR5800SP2E

KEYBOARD enhanced PERSONAL DIGITAL ASSISTANT

ZR-5700
MODEL ZR-5800

CONTENTS

CHAPTER 1. SPECIFICATION 1

CHAPTER 2. HARDWARE DESCRIPTION 4

CHAPTER 3. NOTE FOR SERVICING 29

CHAPTER 4. DISASSEMBLY AND ASSEMBLY 36

CHAPTER 5. DIAGNOSTICS AND CHECK ITEMS 44

CHAPTER 6. CIRCUIT DIAGRAM & PARTS LAYOUT 46

PARTS GUIDE

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

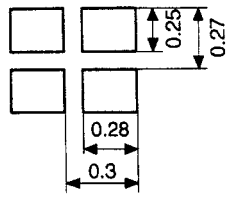
This document has been published to be used for after sales service only.
The contents are subject to change without notice.

CHAPTER 1. SPECIFICATION

DISPLAY SECTION

ELEMENT: DFSTN LCD

DISPLAY: ZR5700
319 × 240 dot matrix liquid crystal display
ZR5800
319 × 240 dot matrix liquid crystal display with Backlight function



(mm)

LSI

CPU: LH5809
PCMCIA CONTROLLER: J6951S
ASIC: LH58171

POWER SUPPLY

AC: O (AC Adapter EA-23E, Battery pack CE-BK1) DC: O
Main power supply: 3 VDC Alkaline batteries (LR6 (AA) × 2)
Memory backup power: 3 VDC lithium battery (CR2032 × 1)

POWER CONSUMPTION

ZR5700: 0.5 W ZR5800: 0.9 W (at Backlight ON)

AUTO POWER OFF TIME

15 minutes

MEMORY PROTECT

Yes

DIMENSIONS

Open: 170 (W) × 191 (D) × 18.0 (H) mm.
Closed: 170 (W) × 100 (D) × 25.4 (H) mm.

Weight

ZR5700: Approx. 380 g (0.84 lb) including batteries
ZR5800: Approx. 390 g (0.86 lb) including batteries

Serial input/output

Type of transmission: Asynchronous half-duplex/fullduplex
Transmission speed: 300, 600, 1200, 2400, 4800, 9600, 14400 bps
Parity bit: even, odd, none
Word length: 7 or 8 bits
Stop bit: 1 or 2 bits
Connector used: 15-pin connector
Output signal level: C-MOS level (5V±10% volts)
Interface signals: Input; RD, CS, CD, DR, CI
Output; SD, RS, RR, ER
Other; SG, VC, FG

Operating temperatures

0°C to 40°C (32° to 104°F)

Peripherals and transfer interface

IR send distance:
- 50 cm (20 inches) maximum at speeds of 9600 bps to 115 kbps using IrDA compatible protocol.
- 50 cm (20 inches) maximum at speeds of 9600 bps to 19.2 kbps using Sharp IR (ASK) protocol.
- IR distance may change depending on the system used.

Cable jack: 15-pin
PCMCIA card slot: 1 (Type II)
DISPLAY: ZR5700 → LF7854Q1
ZR5800 → LF7854S1

Electronic Organizer notebook section

Applications: Activities, Contacts, Data Files, Notes, Documents, Outlines

Desk accessories: Calculator, Spreadsheets, Scrapbook, Filer, Search, Help, Tools and Help

Memory capacity:
ZR5700 1 MB (User area: Approx. 600 KB)
Appointments capacity: Approx. 8,850 entries
Contacts capacity: Approx. 8,600 entries

ZR5800 2 MB (User area: Approx. 1,624 KB)
Appointments capacity: Approx. 25,450 entries
Contacts capacity: Approx. 24,700 entries

These capacities assume the following average entry sizes and only apply whe all the available memory is committed to single function.
Appointements: 32 characters/entry
Contacts: 16 characters/entry in the name field 12 characters/entry in the number field

Maximum data per entry:
Documents: 16 Kbytes
Outlines: 32 Kbytes for an entire outline, 2 Kbytes for each topic
Contacts 2 Kbytes for text data,
Data Files: 61.7 Kbytes for graphics data 2 Kbytes
Others: 2 Kbytes

User interfaces: Touch panel, keyboard

Other features: Secret function, data transfer, keyword search, messages, etc.

Calculator

Digits: 10
Functions: Addition, subtraction, multiplication division; constant, square root, percent, memory calculation, data calculation, paperless printer.

Clock

Crystal frequency: 32,768 Hz
Clock precision: Average variance per day, 1.5 seconds (at 25°C/77°F)
Content of displays: Year, month, day, day of week, hours, minutes, A.M./P.M., city names
Time system: 12-hour and 24-hour clock
Others functions: Date and time for world cities.
Daylight saving time (DST) function.

Operating time

ZR-5700
- 70 hours approx.
2 months of 1 hour per day continuous display at ambient temperature of 23°C (73°F).
- 45 hours approx.
1.5 months of 1 hour per day use, searching data for 5 minutes and display for 55 minutes, at ambient temperature of 23°C (73°F).

ZR-5800
- 70 hours approx.
2 months of 1 hour per day continuous display at ambient temperature of 23°C (73°F).
- 45 hours approx.
1.5 months of 1 hour per day use, searching data for 5 minutes and display for 55 minutes, at ambient temperature of 23°C (73°F).
- 35 hours approx.
1 month of 1 hour per day use, searching data for 5 minutes and display for 55 minutes, with using the Backlight for 2 minutes per hourly use at ambient temperature of 23°C (73°F).

Memory backup:
- 1 month approx. (with depleted operating batteries)
- 5 years approx. (with replacement of depleted operating batteries).

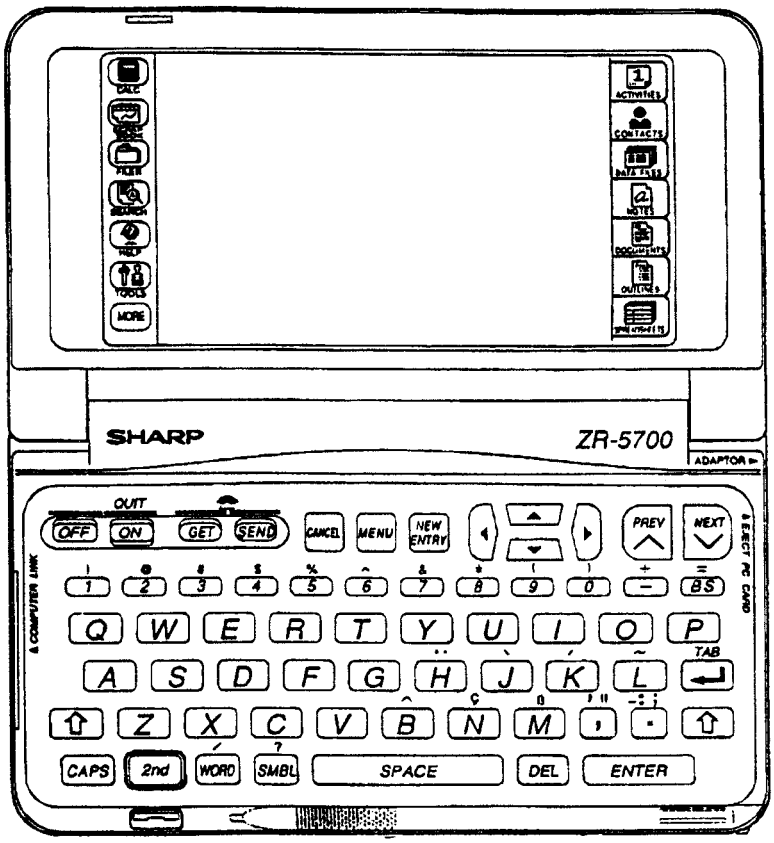
Operating temperature: 32° to 104°F (0° to 40°C)

Accessories

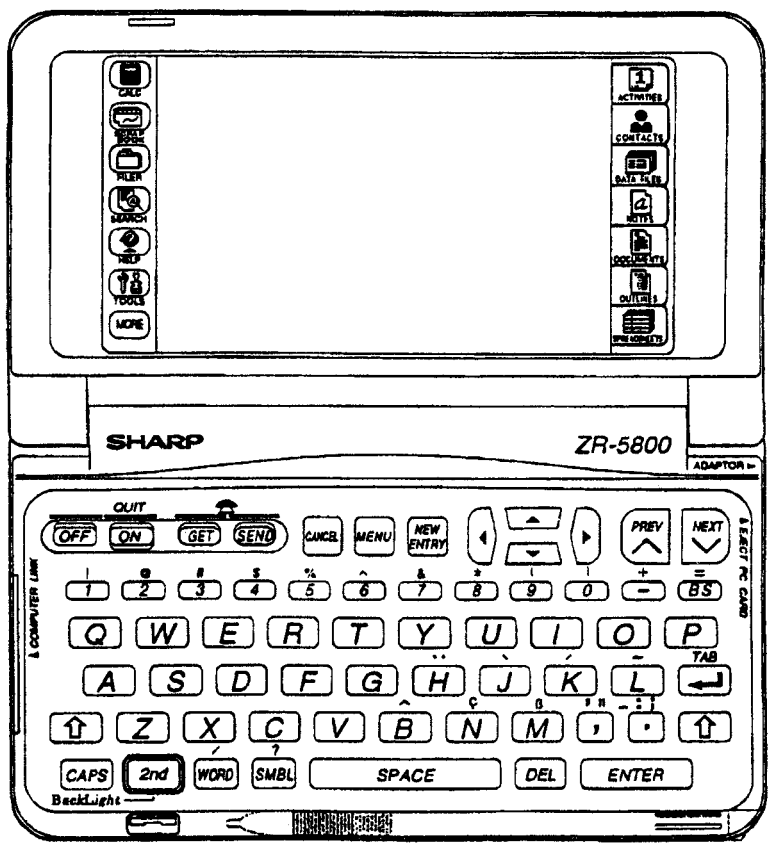
Alkaline batteries (LR6 (AA) × 2)
Lithium batteries CR2032 (installed)
Touch pen, Operation manual, protection card (installed)

KEY LAYOUT

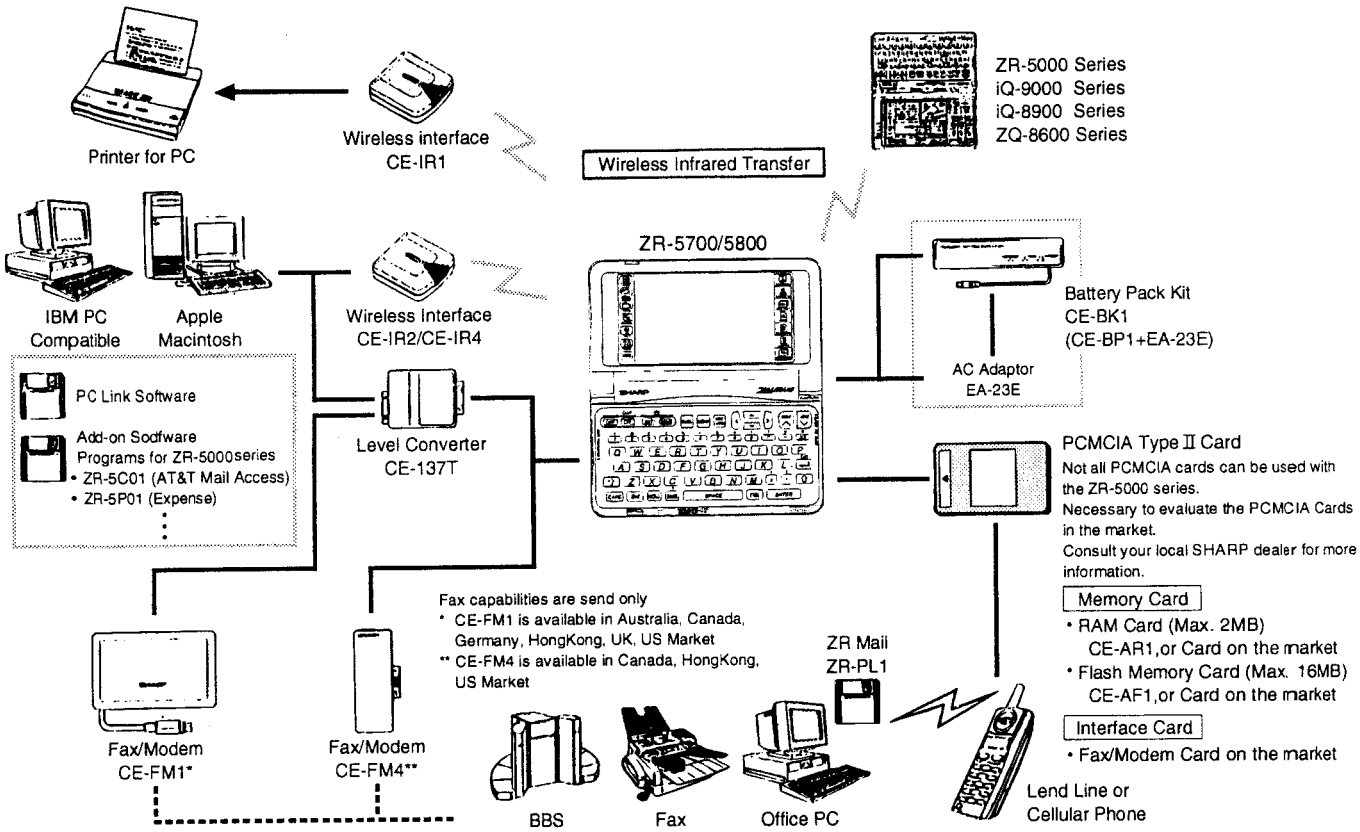
① ZR-5700



② ZR-5800

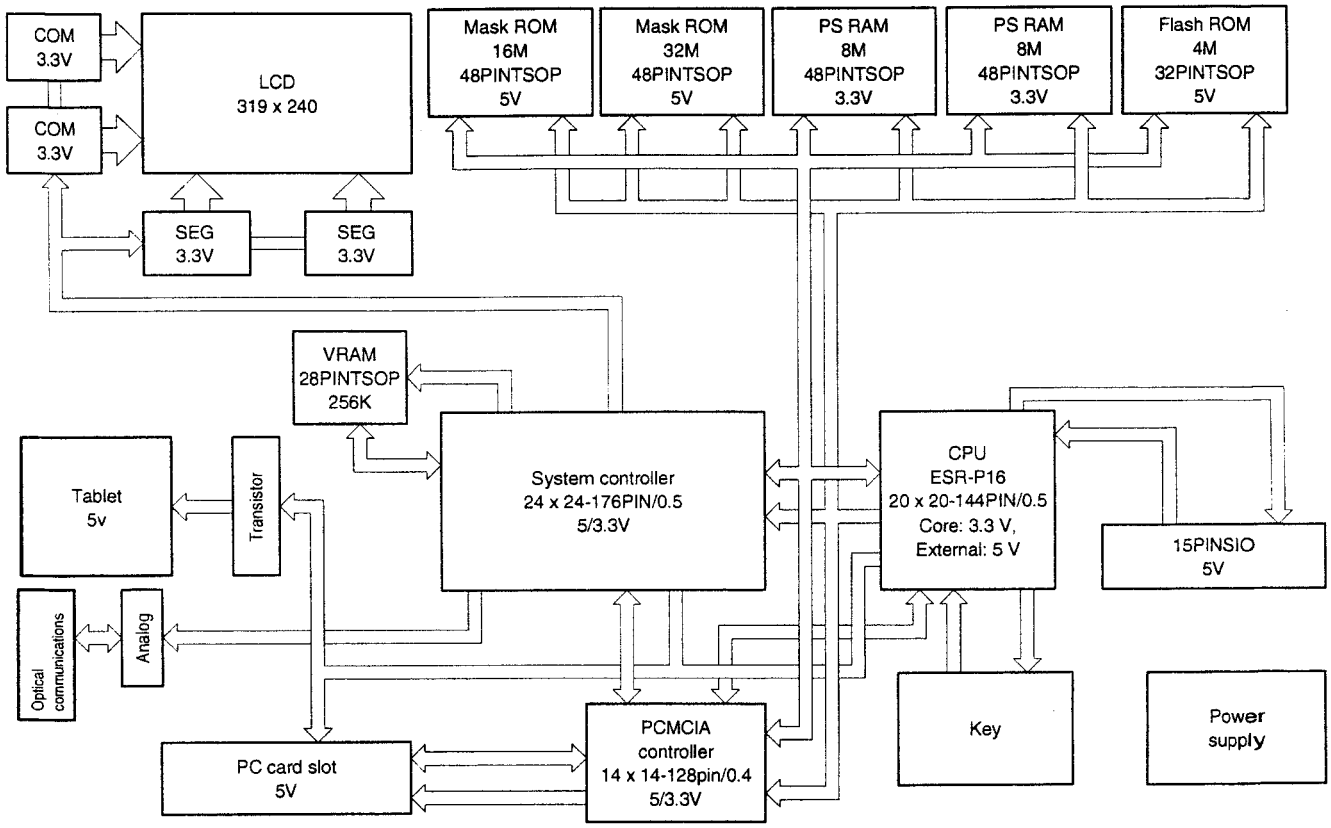


SYSTEM CONFIGURATION



CHAPTER 2. HARDWARE DESCRIPTION

1. BLOCK DIAGRAM



2. SYSTEM DESCRIPTION

2-1. System configuration

The ZR-5700 and 5800 are composed of CPU, PCMCIA controller, system gate array, and memory. The memory uses 16 M + 32 M mask ROM, 8 M PSRAM (2 units), 4 M flash ROM, and 256 KSRAM. Each LSI is outlined as follows:

1) CPU
   Uses the same P16 (LH5809) that is used on the ZR-5000.
2) PCMCIA controller
   Uses the same J6951S that is used on the ZR-5000.
3) System gate array
   The system gate array has built-in LCD controller, and RTC (including A/D converter and voltage detection circuit) random logic block.
4) Memory
   a) ROM
      16 M + 32 M mask ROM will be equipped.
   b) RAM
      One or two units of 8 M PSRAM will be equipped.
   c) Flash
      A 4 M flash ROM will be equipped to patch and download the software.
   d) VRAM
      Uses the same 256 KSRAM that is used on the ZR-5000.
5) Power source
   2 AA alkali-manganese batteries will be used as the main batteries, to raise the voltage to 5 V and 3.3 V. The lithium battery will be used as a backup battery.

3. DESCRIPTION OF LSI

3-1. CPU (LH5809)

1) Outline

(1) CMOS process (P type silicon)

(2) 16 bit us CPU (Operand 8 bit)

(3) Firmware ROM (decoder)

(4) RAM 240 Bytes

(5) Dynamic wait function
Internal setting is possible with external signal control and 0 ~ 7 Wait chip enable unit.

(6) Dynamic bus sizing function
Internal setting is possible with 16 bit → 8 bit bus width selection, external signal control, and chip enable unit.

(7) Bus open function
Open allow/inhibit can be set internally.

(8) I/O port

<Input>	Key input:	8 ports
	System control input:	7 ports
	Memory control input:	2 ports
	Bus control input:	1 port
	UART input:	1 port
	General input (Interrupt signal):	16 ports
<Output>	Key strobe output:	16 ports
	Address output:	24 ports
	Chip enable output:	13 ports
	Memory control output:	8 ports
	Bus control output:	2 ports
	UART output:	1 port
	General output (ICE control signal):	16 ports
	Buzzer output:	1 port
	Sub clock output:	1 port
	System clock output:	1 port
	Main clock output:	1 port
<I/O>	Data I/O:	16 ports
<Others>	Core section power terminal:	2 ports
	I/O external power terminal:	1 port
	GND terminal:	2 ports
	Oscillator terminal:	4 ports

(9) Built-in circuit
Oscillation circuit, main: Ceramic oscillation
sub: CR oscillation
Reset circuit
UART

(10) Power voltage: Core section 2.7 ~ 3.6 (VCC ≦ VIO) [V]
I/O section 2.7 ~ 5.5 (VCC ≦ VIO) [V]

(11) Rated operating temperature: 5 ~ +55 [°C]

(12) Not a bit slice microprocessor.

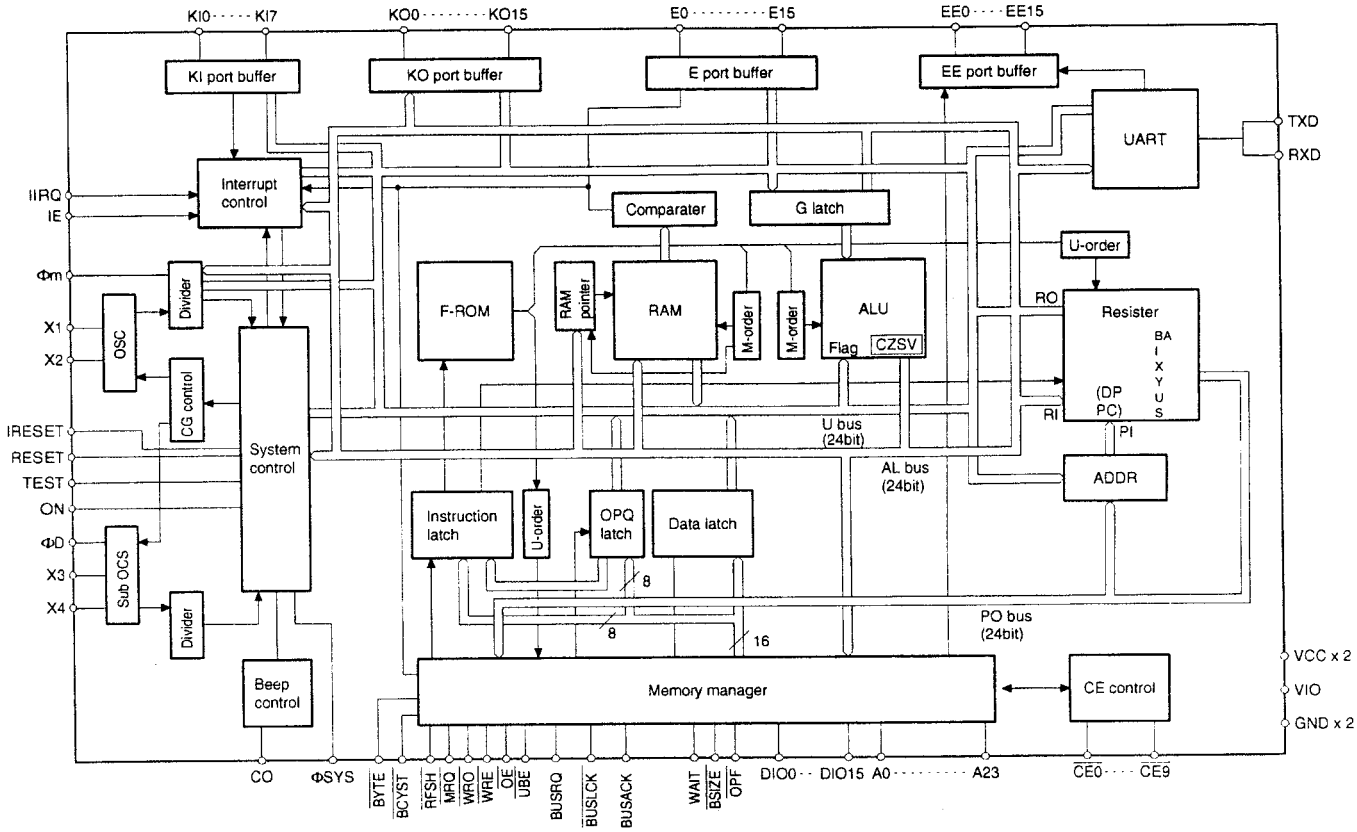
(13) Multiplication function is not available.

(14) ROM type memory element is not included.

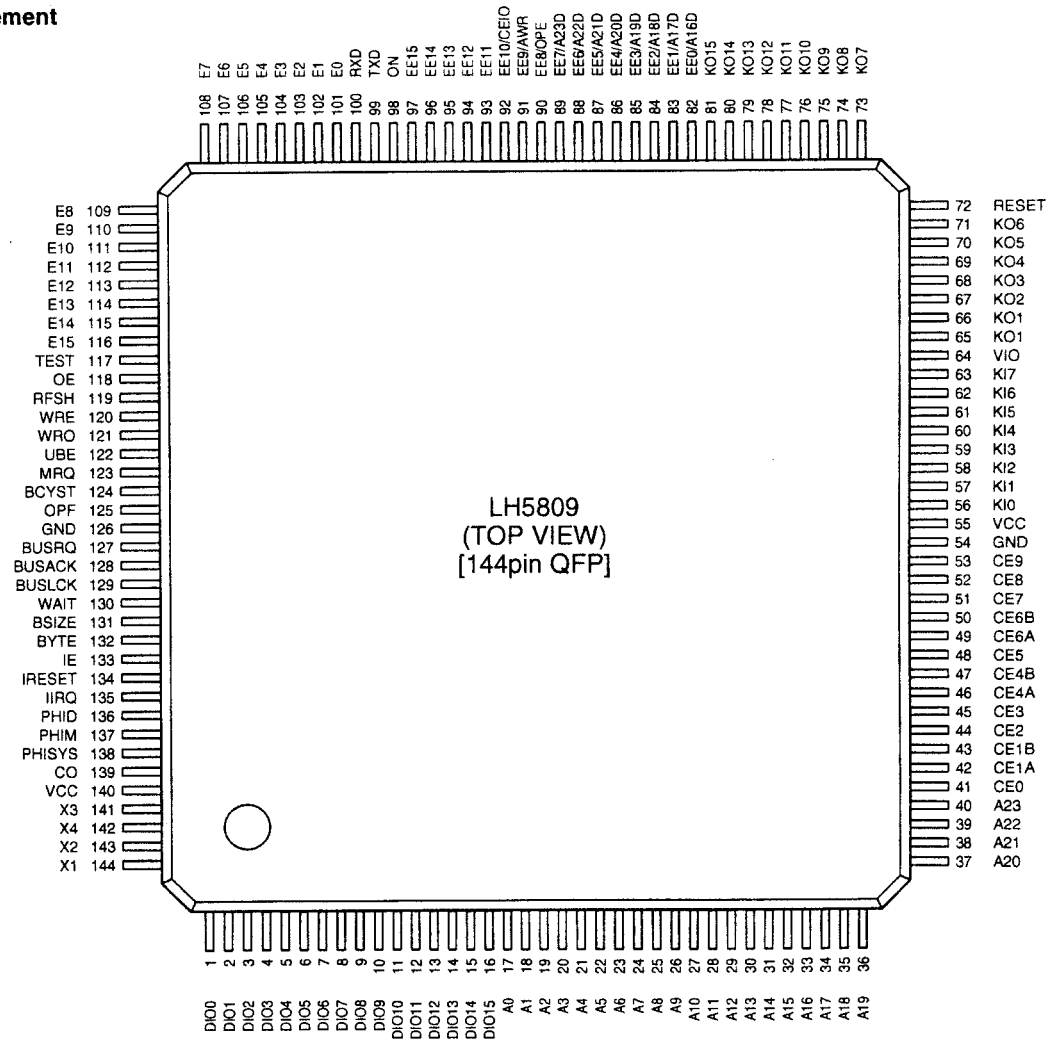
(15) 144 pin TQFP (plastic package)

(16) No radiation-proof design.

2) Block diagram



1) Pin arrangement



4) Pin name

No.	Pin name	Function
1~16	DIO 0~15	I/O buffer (TTL) with pull-up resistor
17~40	A 0~23	Tri-state output buffer with pull-down resistor
41~53	-CE 0~9	Tri-state output buffer with pull-up resistor
54, 126	GND	GND pad
55, 140	VCC	Internal 3V power source
56~63	KI 0~7	Input buffer with pull-down resistor
64	VIO	Output buffer 5V power source
65~71, 73~81	KO 0~15	Key output buffer
72	RESET	Schmidt trigger input buffer with pull-down resistor
82~97	EE0~15 (ICE-MODE)	Output buffer (CMOS)
98	ON	Schmidt trigger input buffer with pull-down resistor
99	TXD	Output buffer (CMOS)
100	RXD	Input buffer with pull-down resistor
101~116	E 0~15	Input buffer with pull-down resistor
117	TEST	Schmidt trigger input buffer with pull-down resistor
118	-OE	Tri-state output buffer with pull-up resistor
119	-RFSH	Tri-state output buffer
120	-WRE	Tri-state output buffer with pull-up resistor
121	-WRO	Tri-state output buffer with pull-up resistor
122	-UBE	Tri-state output buffer with pull-up resistor
123	-MRQ	Tri-state output buffer with pull-up resistor
124	-BCYST	Tri-state output buffer with pull-up resistor
125	-OPF	Tri-state output buffer with pull-up resistor
127	BUSRQ	Input buffer
128	BUSACK	Output buffer (CMOS)
129	-BUSLCK	Output buffer (CMOS)
130	WAIT	Input buffer
131	BSIZE	Input buffer
132	-BYTE	Input buffer
133	IE	Input buffer
134	IRESET	Schmidt trigger input buffer with pull-down resistor
135	IIRQ	Input buffer
136	φD	Output buffer (CMOS)
137	φM	Output buffer (CMOS)
138	φSYS	Output buffer (CMOS)
139	CO	Output buffer (CMOS)
141	X3	Oscillator buffer (Sub, CR oscillation TYP40KHz)
142	X4	Oscillation circuit input buffer (Sub)
143	X2	Oscillation circuit input buffer (Main)
144	X1	Oscillator buffer (Main, crystal oscillation 9.216MHz)

(Note) E0~E3 and E9 have no pull-down resistor.

A0~23:	Address bus
DI00~15:	Data bus
CE0~9 (13 lines):	Chip select output
WRE,WRO,OE:	Memory control
KI0~7, KO0~15:	Key strobe input/output
E0~15:	Versatile-use input port (Can be used as an external interrupt pin.)
EE0~15:	Versatile-use output port
RXD, TXD:	UART data input/output
ON key:	ON key input

5) CPU port allocation table

Signal	Allocation (inside the CPU)	Condition
DIO0	Lower data bus (PU)	
DIO1	Lower data bus (PU)	
DIO2	Lower data bus (PU)	
DIO3	Lower data bus (PU)	
DIO4	Lower data bus (PU)	
DIO5	Lower data bus (PU)	
DIO6	Lower data bus (PU)	
DIO7	Lower data bus (PU)	
DIO8	Upper data bus (PU)	
DIO9	Upper data bus (PU)	
DIO10	Upper data bus (PU)	
DIO11	Upper data bus (PU)	
DIO12	Upper data bus (PU)	
DIO13	Upper data bus (PU)	
DIO14	Upper data bus (PU)	
DIO15	Upper data bus (PU)	
A0	Address output (PD)	
A1	Address output (PD)	
A2	Address output (PD)	
A3	Address output (PD)	
A4	Address output (PD)	
A5	Address output (PD)	
A6	Address output (PD)	
A7	Address output (PD)	
A8	Address output (PD)	
A9	Address output (PD)	
A10	Address output (PD)	
A11	Address output (PD)	
A12	Address output (PD)	
A13	Address output (PD)	
A14	Address output (PD)	
A15	Address output (PD)	
A16	Address output (PD)	
A17	Address output (PD)	
A18	Address output (PD)	
A19	Address output (PD)	
A20	Address output (PD)	
A21	Address output (PD)	
A22	Address output (PD)	
A23	Address output, not used (PD)	Open
–CE0	Not used (PU)	Open
–CE1A	Machine body RAM select (PU)	
–CE1B	Machine body RAM select (PU)	
–CE2	Not used (PU)	Open
–CE3	PCMCIA memory select (PU)	
–CE4A	Not used (PU)	Open
–CE4B	Not used (PU)	Open
–CE5	Not used (PU)	Open
–CE6A	Machine body ROM select (PU)	
–CE6B	Machine body ROM select (PU)	
–CE7	I/O select (PU)	
–CE8	Not used (PU)	Open
–CE9	Not used (PU)	Open
KI0	Key input (PD)	
KI1	Key input (PD)	
KI2	Key input (PD)	
KI3	Key input (PD)	
KI4	Key input (PD)	
KI5	Key input (PD)	
KI6	Key input (PD)	
KI7	Key input (PD)	
KO0	Key strobe	
KO1	Key strobe	
KO2	Key strobe	
KO3	Key strobe	
KO4	Key strobe	
KO5	Key strobe	
KO6	Key strobe	
KO7	Key strobe	
KO8	Key strobe	
KO9	Key strobe	
KO10	Key strobe	
KO11	Backlight presence detection strobe	
KO12	RAM capacity detection	
KO13	Flash/EE detection	
KO14	??? detection strobe (spare)	
KO15	Low-voltage card detection strobe	
E0	Tablet interrupt	Pull down
E1	Lock interrupt	Pull down
E2	Low-voltage card detection 1	PU to K015
E3	Low-voltage card detection 2	PU to K015
E4	Card interrupt (PD)	
E5	PC controller interrupt (PD)	
E6	Alarm interrupt (PD)	
E7	Reservation (PD) and recognition interrupt	Open
E8	Various initial settings reading (PD)	
E9	AC adapter detection	
E10	15-pin CD (PD)	
E11	15-pin DR (PD)	
E12	15-pin CS interrupt (PD)	
E13	15-pin CI interrupt (PD)	
E14	Detection of LCDC's LP (PD)	
E15	Not used (PD)	
EE0	LVC power down & card detection	
EE1	Dummy load	
EE2	12 V control - 1	
EE3	12 V control - 2, via INV	
EE4	SLEEP (PC controller)	
EE5	PC controller reset	
EE6	Machine body VPP 12 V ON	
EE7	Card VPP 12 V ON	
EE8	Card VPP 5 V ON	
EE9	Dummy load	
EE10	Machine body flash power down	
EE11	Factory-set circuit data & IR issuance control	
EE12	15-pin SELECT	
EE13	15-pin RS	
EE14	15-pin ER	
φIR	Clock for IRDA	
TXD	Serial output	

Signal	Allocation (inside the CPU)	Condition
RXD	Serial input (PD)	
ON	ON key input (PD)	
OE	Pass lead (PU)	
–RFRH	Memory non-access (PU)	Open
–WRE	Even-numbered address write (PU)	
–WRO	Odd-numbered address write (PU)	
–MRQ	Memory cycle (PU)	
–BCYST	Bus cycle start (PU)	Open
OPF	Operation fetch cycle	Open
WAIT	Wait input	
BSIZE	Bus width control input	
BUSRQ	Bus request	
BUSACK	Response to bus request	
–BUSLCK	Bus lock	Open
φSYS	System clock output	
φM	Main clock output	
φD	Sub-clock output	
–UBE	Upper byte access (PU)	
–BYTE	Bus width set during reset	HIGH
CO	Buzzer output	
RESET	Reset input (PD)	
X1	Cell lock output	Oscillator
X2	Cell lock input	Oscillator
X3	CR oscillation output	Resistor
X4	CR oscillation input	Resistor
IE	ICE enable	GND
IRESET	ICE reset	GND
IIRQ	ICE interrupt	GND
TEST	Test terminal (PD)	GND

3-2. ASIC

1. Product outline

The LH58171 is a controller designed for use with the ZR-5700 and 5800.

Configuration: 10-bit A/D converter, voltage detection circuit, 32 KHz oscillation circuit, and 50 K gate array

Function/Application: Controller for the ZR-5700/5800

2. Terminal allocation

Pin No.	I/O	Signal	Pin No.	I/O	Signal	Pin No.	I/O	Signal	Pin No.	I/O	Signal
1	—	VIO	45	—	GND	89	TO5	BSIZE	133	O3	DIS
2	I/O5	A0	46	Iosc	OSCI	90	I5	CE1A	134	O3	FRM
3	I/O5	A1	47	Oosc	OSCO	91	I5	CE1B	135	O3	YD
4	I/O5	A2	48	—	GND	92	TO5	CE3	136	O3	LP
5	I/O5	A3	49	Ireg	VREG	93	I5	CE6A	137	O3	XCK
6	I/O5	A4	50	Ivdt	VD0	94	I5	CE6B	138	O3	SD0
7	I/O5	A5	51	Ivdt	VD1	95	I5	CE7	139	O3	SD1
8	I/O5	A6	52	Ivdt	VD2	96	Is	CI	140	O3	SD2
9	I/O5	A7	53	Ivdt	VD3	97	TO5	PB20N	141	O3	SD3
10	I/O5	A8	54	Is	ONKEY	98	O5	OPTS	142	—	VCC
11	I/O5	A9	55	Is	RSKEY	99	I5	OPTR1	143	O3	AX0
12	I/O5	A10	56	Is	BTCOV	100	I5	OPTR2	144	O3	AX1
13	I/O5	A11	57	I5	VREF	101	I5	RD	145	O3	AX2
14	I/O5	A12	58	Ivin	VIN0	102	O5	SD	146	O3	AX3
15	I/O5	A13	59	Ivin	VIN1	103	O5	ALRMO	147	O3	AX4
16	I/O5	A14	60	Iavd	AVDD	104	O5	BELLO	148	O3	AX5
17	I/O5	A15	61	TO5	SWAN	105	TO5	VR1	149	O3	AY0
18	—	GND	62	TO5	MON	106	TO5	VR2	150	O3	AY1
19	I/O5	A16	63	TO5	YMONN	107	TO5	VR3	151	O3	AY2
20	I/O5	A17	64	TO5	XMONN	108	I/05	VR4	152	O3	AY3
21	I/O5	A18	65	TO5	SWYIIN	109	I/05	VR5	153	O3	AY4
22	I/O5	A19	66	TO5	SWXIIN	110	I/05	VR6	154	O3	AY5
23	I/O5	A20	67	TO5	SWYL	111	I/05	BLON	155	O3	AY6
24	I/O5	A21	68	TO5	SWXL	112	—	GND	156	O3	AY7
25	I/O5	A22	69	—	GND	113	Is	UNLOCK	157	—	GND
26	TO5	EPA7	70	I/05	D0	114	O5	SHIPSET	158	Ick	XC2
27	TO5	EPA8	71	I/05	D1	115	O5	ON	159	Ock	XC1
28	TO5	EPA13	72	I/05	D2	116	O5	RESETO	160	—	VCC
29	TO5	EPA14	73	I/05	D3	117	I5	EE11	161	I5	BSZPC
30	TO5	EPA15	74	I/05	D4	118	I5	VEEFB	162	I5	WTPC
31	TO5	EPA16	75	I/05	D5	119	O5	VEECLK	163	I5	MREQ
32	—	VIO	76	I/05	D6	120	O5	CK32II	164	I/05	WRE
33	O5	CEEPN	77	I/05	D7	121	—	VCC	165	I/05	WRO
34	O5	EPRSN	78	—	VIO	122	I/O3	LDIO0	166	I/05	OE
35	TO5	WREP	79	I/05	D8	123	I/O3	LDIO1	167	I/05	UBE
36	O5	OERFSH	80	I/05	D9	124	I/O3	LDIO2	168	I5	PHIIR
37	O5	CEPS1N	81	I/05	D10	125	I/O3	LDIO3	169	I5	TXD
38	O5	CEPS2N	82	I/05	D11	126	I/O3	LDIO4	170	O5	RXD
39	TO5	ROMBN	83	I/05	D12	127	I/O3	LDIO5	171	O5	WAIT
40	TO5	ROMAN	84	I/05	D13	128	I/O3	LDIO6	172	O5	BUSRQ
41	I5	BZIN	85	I/05	D14	129	I/O3	LDIO7	173	I5	PHIM
42	Is	ALLRESET	86	I/05	D15	130	TO3	LCE	174	I5	BUSACK
43	Is	TEST	87	—	GND	131	TO3	LRW	175	I5	PHISYS
44	O5	VDET10	88	O5	BZOUT	132	—	GND	176	—	GND

I/O5 : 5 V input and output
I5 : 5 V input
O5 : 5 V output
I/O3 : 3 V input and output
I3 : 3 V input
O3 : 3 V output
Is : 5 V Schmidt input

Iosc : 32 KHz oscillation input
Oosc : 32 KHz oscillation output
Ick : 8 MHz oscillation input
Ock : 8 MHz oscillation output
TO5 : 5 V triad state output
TO3 : 3 V triad state output

3. System gate array

The ZR-5700 and 5800 have the RTC and LCDC blocks incorporated inside their system gate array. Although the respective functions of these blocks retain compatibility with those used on the ZR-5000, some functions have different specifications.

1) LCDC block

a) Connection
The LCDC mode settings, which used to be made using an external terminal, are now fixed inside the gate alley as follows:

Segment data bus width:	4 bits
No. of graphical dots:	320 × 240
Tone:	2 tones (monochrome)
Oscillation system:	Self-oscillation by ceramic oscillator
System data bus width:	8 bits

2) RTC block (including A/D converter)

All the circuits, except for the voltage detector and A/D converter, are compatible with the SMC5248; refer to the ZR-5000 service manual.

a) Voltage detectors
Since the voltage detection circuit of this ASIC system consumes greater amount of current than the SMC5248, the detection circuit is equipped with an intermittent detection system, in addition to the conventional detection system.

Intermittent mode resistor

bit1	bit0	Function
0	0	Detector A always ON
0	1	Detector A1/8 ON
1	0	Detector A1/64 ON
1	1	Detector A always ON

1/8 = 2mS/16mS
1/64 = 2mS/128mS

When the set is operating, the detector is always ON, whereas when the set is OFF, the detector is performing intermittent detection (1/64).

- Detector B (VD 1, 2 and 3 terminals)
  Same as the SMC5248.
- Detector C (VIO terminal)
  Performs detection at the intermittence of 1/128.

4. Gate array block

Equivalent to the system gate array of the ZR-5000, this block is equipped with the following functions.

1) Protection by VDET10 signal

The VDET10 signal monitors the logic power voltage (5 V).
It becomes "L" if the voltage drops and stays below the specified voltage level (i.e., the preset voltage level for the detector C of the RTC block) for about 200 msec. If this signal stays "L" for about 60 msec, the gate alley will put all of the outputs into non-active or Hi-z state, while making the inputs non-active.
To disable the hardware protection, replace the batteries and press the battery replacement switch. (Be aware that the hardware protection can not be disabled if the voltage of the new batteries is low.)

2) Protection of pseudo-SRAM

Should the hardware protection function be actuated while the pseudo-SRAM is being accessed - such as when the batteries are taken out during its operation - the operation cycles will only remain effective that have been accessed before the protection function was actuated. When the access is over, the chip select function of the pseudo-SRAM is made non-active.

3) Protection of flash memory

The flash memory, to which the patch software is written to cope with software bugs, is given various protective measures.

- Write-protection
  The write-protection function can not be disabled unless VPP 12 V is supplied through the EE2 and EE6 ports. To disable this function, add 0AXH and 05XH consecutively to 1F8B05H. This outputs the write signal WREP. (X signifies DON'T CARE.
  The setting is held at "H" when the protection is effective.)

4) Optical communications function

This function supports two systems: the DASK system and the IRDA system.
To reduce power consumption, the PB20N is usually held at Hi-z.

5) Pseudo-SRAM refresh function

The pseudo-SRAM refresh function can be set either to the automatic refresh mode or to the self-refresh mode, by changing the resistor settings inside the gate array. Should insufficient refresh operation occur, the CPU gets interrupted, and should unusual operations occur, the CPU gets reset, to prevent the pseudo-SRAM memory from becoming garbled.

a) Specifications

i) At the time of insufficient refresh operation: Should the refresh function fail to complete 2,048 times of refresh operation within 14 msec (measured by dividing PHIM), the error flag is set (1F8B1CH bit = "1"), to trigger interrupt signals inside the CPU (ALRMO = "1"). The flag is released by the hardware after the refresh operation is complete.

ii) At the time of unusual operations In case of the occurrence of the following problems, the CPU gets reset (RESETO = "1"), and the gate alley is totally initialized. If the refresh function still fails to complete the 2,048 times of refresh operation in 7 more msec after the time stated in item i above) has elapsed (total 21 msec). If the pseudo-SRAM is accessed during the refresh operation.

6) Dynamic bus sizing

The CPU, which is designed to carry out 16-bit access, can also execute 8-bit access by dynamically controlling the bus width inside the gate alley. 8-bit access is executed by setting the BSIZE signal for the CPU to "L". The dynamic bus sizing takes place in the following conditions. It should be noted here that should the CPU fail to access the upper bytes (D8 thru D15), bus sizing will not take place.

a) During access to the RTC and LCDC blocks

b) During access to the PCMCIA controller

c) When a request for bus sizing has been made from the PCMCIA (BSZPC = "L")

d) During access to the flash ROM (including the hardware hook)

7) Wait control

The PENGUIN 2 system is designed to execute all the accesses at a single wait. It is also designed so that multiple waits are available from outside the system. Wait is enabled when the WAIT signal is set to "1" in the CPU. Wait takes place in the following conditions:
During the period that the busy signal is set to "1" in the LCDC block, and when a request for wait has been made from the PCMCIA (WTPC = "1")

8) Tablet

As with the PENGUIN system, control is executed by the bits 0 thru 7 for 1F8B04H. Normally, with only the MON signal set to "1," when the tablet is pressed, an "H" level signal is fed through the CPUs E0 port, thereby enabling interrupt. When using the A/D converter, the SWAN signal is set to the "L" level, to supply the A/D converter with reference voltage.

9) Clock

a) From the CPU, the following frequencies should be supplied.
- 9 MHz to PHISYS
- 3 MHz to PHIM
- 1.8 MHz to PHIIR (for the IRDA system only)

b) Clock for A/D converter
The clock for the A/D converter is supplied by dividing the PHISYS into four equal parts and then by setting the bit 1 for 1F8B00H to "1". Since at present the A/D converter's operational margin remains undetermined, this clock is designed for the time being so that setting the bit 3 for 1F8B2EH to "1" switches the division to two halves of the PHIM.

c) Clock for raising power voltage for LC
As the clock for raising voltage, 32 KHz is output from the RTC block to the VEECLK when the VEEFB (feedback signal from the pressure rise circuit) is held at "H."

10) Others

a) Factory-set circuit
Unlike the PENGUIN system to which the factory-set circuit was connected externally, this system has the circuit built into it. The data line uses the CPU's EE11 port, and the clock uses the write signal for the flash ROM. The preset output is fed as the SHIPSET signal from the gate alley. It should be noted that the reset signals (triggered by the reset key, battery replacement switch, etc.) do not release the SHIPSET signal.

b) ON factor masking
The ON factors - ON key, alarm, and 15-pin CI - are masked so that they will not be output to the CPU during battery placement and card lock release, and under less-than-fatal level conditions, thereby preventing malfunctions.

3-3. PCMCIA CONTROLLER (J6951S)

1) Introduction

The J6951S is the PC card (memory card or I/O card) controlling LSI which conforms to the world standards, JEIDA Ver.4.1 and PCMCIA Release 2.0.
A variety of functions including wait control and interruption control facilitate designing of the PC card interface system of the host system.

2) Features

The major features of the J6951S are described below.

① Host bus interface

- Memory window
Memory on the PC card can be mapped to the window of 1MB × 2 pages and 16KB × 4 pages in the host memory address.
The lower 14 bits of each address of 16KB host window start with 0. The size of memory which the J6951S can handle is 2MB in the host side and max. 64MB in the card side.
- I/O window
The PC card I/O address is assigned straight to the I/O space (32KB) of the host.
The size of I/O which the J6951S can handle is 32KB in the host side and max. 64KB in the card side.
- Programmable wait control
The number of wait can be set for I/O access.
- Interruption
Interrupt request from the PC card and interrupt request generated in the J6951S are separately outputted.
- Sleep mode
By setting the J6951S to the sleep mode, signals in the host bus side can be separated. This reduces the current consumption of the system.

② Card interface

- Supports memory cards and I/O cards of JEIDA Ver.4.1 and PCMCIA Release 2.0 specifications.
- When access is not made to the card, the bus in the card side can be fixed to LOW.
- One J6951S supports one slot.

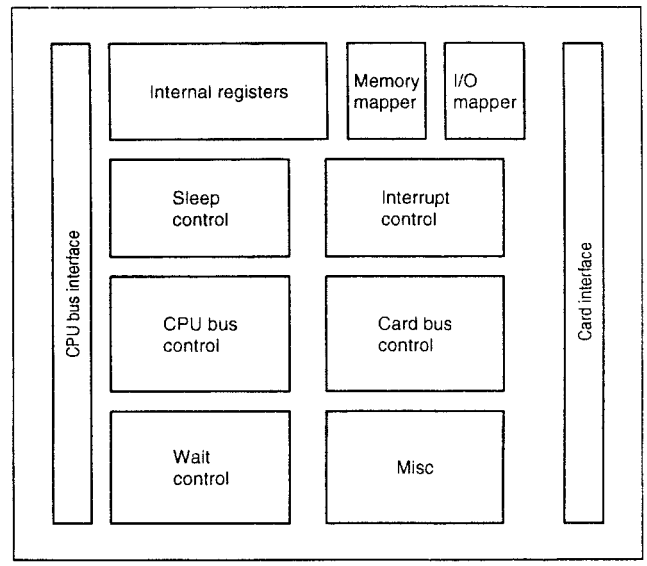
③ Additional features

- The card state can be monitored with the register content.
- By changing the card state, an interruption can be generated.

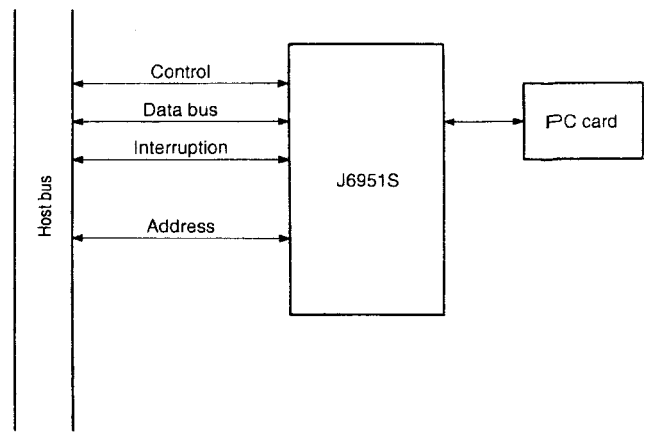
④ Chip specifications

- The chip operates on 3.3V.
- The CPU bus operates on 5V, and the PC card bus operates on 5V or 3.3V according to the PC card power source.
- The package of 128 pin plastic QFP is employed.

3) Block diagram



4) System composition



5) Pin functions

① CPU bus signals

Pin name	I/O	Function
SD0–SD15	B	System data bus (16 bit bi=directional data bus)
SA0–SA20	I	System address bus
IRQ	O	Interruption signal generated by the J6951S. Interruption request at HIGH.
PCIRQ	O	Interruption signal generated by the PC card. Interruption request at HIGH.
SLEEP#	I	Hardware sleep signal. Sleep mode at LOW. When this signal is LOW, the J6951S is in the hard sleep mode and all output pins except for PCIRQ and IRQ are Hi-Z.
RESET#	I	Reset signal. Reset at LOW.
BHE#	I	Driven to LOW when an access is made through the upper byte (SD8-15) of the data bus is made.
CLK	I	System clock 9.216MHz
MREQ#	I	Card memory selection signal. Driven to LOW when the system makes an access to 400000h ~ 5FFFFFh (2MB). The 2MB area of 400000h ~ 5FFFFFh can be used only by the J6951S. In a read cycle, data are latched at the rising edge of MREQ#.
IOREQ#	I	I/O selection signals. Driven to LOW when the system makes an access to 1F0000h ~ 1FFFFFh (64KB). The 64KB area of 1F0000h ~ 1FFFFFh can be connected to other I/O devices as well as the J6951S. The I/O card is mapped to 32KB area of 1F0000h ~ 1F7FFFh, and the J6951S register to 1F8800h ~ 1F8802h. In a read cycle, data are fetched at the rising edge of IOREQ#.
RD#	I	Shows that an access to the memory or I/O is read.
CS16	O	Bus sizing signal. HIGH when in 16 bit access, and LOW when in 8 bit access. When no access is made to the J6951S, HIGH is outputted in an access to the memory card. LOW only when 8 bit access is made to the IO card or an access is made to the internal register of the J6951S.
WAIT	O	Wait request signal to the system. When the WAIT signal is HIGH, the access cycle is extended by one cycle of CLK.
AUDIO	O	Digital signal for the speaker.
CPON#	O	When the card power control pin CPON# is LOW, the card power is assumed to be turned on. Controlled by INDEX#40h bit 0. As shown in the table below, this bit is linked with the card signal mode selection as well as CPON#. Index#40h bit 0 — Card signal mode — CPON# L — Shut-down state — H (Card power OFF) H — Access allowed — L (Card power ON) By configuring the system so that LOW state of CPON# is added to the conditions of the card power ON, there is no contradiction with the card power and the card signals. The shut-down state means Hi-Z state of the output pins and the output pins in the internal circuit.

(Note) B: Bidirectional
I : Input
O: Output

② PC card bus signals

Pin name	I/O	Function
CD0–15	B	Card data bus (16 bit bidirectional card data bus)
CA0–25	O	Card address bus
CMEMRD#	O	Card memory read signal
CMEMWR#	O	Card memory write signal
REG#	O	Attribute memory selecting signal. also LOW during an access to the I/O card.
CRESET	O	Card reset
CIORD#	O	Card I/O read
CIOWR#	O	Card I/O write
CE1#	O	Card enable 1
CE2#	O	Card enable 2
CD1#	I	Card detection 1
CD2#	I	Card detection 2 When both card detection 1 and card detection 2 are LOW, the J6951S judges that a card is inserted.
BVD1	I	Battery Voltage Detect 1
BVD2/SPKR#	I	Battery Voltage Detect 2 (Memory card), SPeaKeR (I/O) card)
WP/IOIS16#	I	Write Protect (Memory Card), IOIS16 (I/O Card)
RDY/BUSY#, IRQ#	I	Ready-Busy# (Memory Card), Interrupt Request# (I/O Card)
CWAIT#	I	Wait signal from the card

(Note) B: Bidirectional
I : Input
O: Output

③ Other signals

Pin name	I/O	Function
LVDD	—	Power source for the internal logic circuit and the input PAD. Supplies 3.3V.
SVDD	—	Power source for the output PAD in the CPU signals. Supplied 5.0V.
CVDD	—	Power source for the output PAD in the PC card signals. Supplies 5.0V.
VSS	—	GND
TEST	I	Test pin. Pulled down internally. No connection. May be connected to GND.
N.C.	—	Not connected to the chip. No connection required.

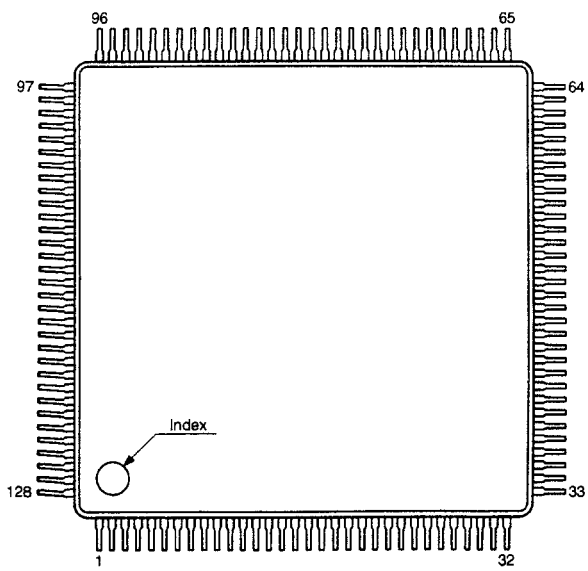
6) Pin name

No	Pin Name	I/O	Power Designator
1	PCIRQ	O	SVDD
2	IRQ	O	SVDD
3	SD0	B	SVDD
4	SD1	B	SVDD
5	SD2	B	SVDD
6	VSS	P	—
7	SD3	B	SVDD
8	SD4	B	SVDD
9	SD5	B	SVDD
10	SD6	B	SVDD
11	SD7	B	SVDD
12	SD8	B	SVDD
13	SD9	B	SVDD
14	SD10	B	SVDD
15	SD11	B	SVDD
16	LVDD	P	—
17	SD12	B	SVDD
18	SD13	B	SVDD
19	SD14	B	SVDD
20	SD15	B	SVDD
21	SA0	I	SVDD
22	SVDD	P	—
23	SA1	I	SVDD
24	SA2	I	SVDD
25	VSS	P	—
26	SA3	I	SVDD
27	SA4	I	SVDD
28	SA5	I	SVDD
29	SA6	I	SVDD
30	SA7	I	SVDD
31	SA8	I	SVDD
32	SA9	I	SVDD
33	SA10	I	SVDD
34	SA11	I	SVDD
35	SA12	I	SVDD
36	SA13	I	SVDD
37	SVDD	P	—
38	SA14	I	SVDD
39	SA15	I	SVDD
40	VSS	P	—
41	SA16	I	SVDD
42	SA17	I	SVDD
43	SA18	I	SVDD
44	SA19	I	SVDD
45	SA20	I	SVDD
46	CD1#	I	SVDD
47	N.C.	N.C.	—
48	CD3	B	CVDD
49	LVDD	P	—
50	CD11	B	CVDD
51	CD4	B	CVDD
52	CD12	B	VCDD
53	CD5	B	CVDD
54	VSS	P	—
55	CD13	B	CVDD
56	CD6	B	CVDD
57	CVDD	P	—
58	CD14	B	CVDD
59	CD7	B	CVDD
60	CD15	B	CVDD
61	CE1#	O	CVDD
62	CE2#	O	CVDD
63	CA10	O	CVDD
64	CMEMRD#	O	CVDD
65	CIORD#	O	CVDD
66	CA11	O	CVDD
67	VSS	P	—
68	CIOWR#	O	CVDD
69	CA9	O	CVDD
70	CA17	O	CVDD
71	CA8	O	CVDD
72	CA18	O	CVDD
73	CA13	O	CVDD
74	CA19	O	CVDD
75	CA14	O	CVDD
76	CA20	O	CVDD
77	CMEMWR#	O	CVDD
78	CA21	O	CVDD
79	RDY/BUSY#, IRQ#	I	CVDD
80	CA22	O	CVDD
81	LVDD	P	—
82	VSS	P	—
83	CVDD	P	—
84	CA16	O	CVDD
85	CA23	O	CVDD
86	CA15	O	CVDD
87	CA24	O	CVDD
88	CA12	O	CVDD
89	CA25	O	CVDD
90	CA7	O	CVDD
91	CA6	O	CVDD
92	CRESET	O	CVDD
93	CA5	O	CVDD
94	CWAIT#	I	CVDD
95	CA4	O	CVDD
96	CA3	O	CVDD
97	VSS	P	—
98	REG#	O	CVDD

No	Pin Name	I/O	Power Designator
99	CA2	O	CVDD
100	BVD2/SPKR#	I	CVDD
101	CA1	O	CVDD
102	BVD1	I	CVDD
103	CA0	O	CVDD
104	CVDD	P	—
105	CD8	B	CVDD
106	CD0	B	CVDD
107	CD9	B	CVDD
108	CD1	B	CVDD
109	CD10	B	CVDD
110	CD2	B	CVDD
111	WP/IOIS16#	I	CVDD
112	N.C.	N.C.	—
113	CD2#	I	SVDD
114	LVDD	P	—
115	CPON# (PC CONT)	O	SVDD
116	AUDIO	O	SVDD
117	WAIT	O	SVDD
118	CS16	O	SVDD
119	VSS	P	—
120	TEST	I	SVDD
121	RD	I	SVDD
122	IOREQ#	I	SVDD
123	MREQ#	I	SVDD
124	CLK	I	SVDD
125	SVDD	P	—
126	BHE#	I	SVDD
127	RESET#	I	SVDD
128	SLEEP#	I	SVDD

B : Bidirectional
I : Input
O : Output P: Power

7) External view of package



8) Appendix

① Output pin state in hard sleep mode (SLEEP# pin at LOW)

In the hard sleep mode, the output pin states are as follows:
These states, however, are observed when the unit is not in the standby mode (card side signals shut-down). For the states in the standby mode, refer to A.2.
The state of the hard sleep mode together with the standby mode occurs in the following three cases:

- When the SLEEP# pin is driven to LOW (to enter the hard sleep mode) in the standby mode.
- When a card is ejected (at least one of CD1# and CD#2 is driven to HIGH) in the hard sleep state.
- When resetting is performed (RESET# is driven to LOW) in the hard sleep state.
- CPU side

Pin name	I/O	State
SD[15:0]	B	Hi-Z
CS16	O	High
WAIT	O	Reversed value of CWAIT#
CPON# (PC CONT)	O	Not affected by SLEEP# pin. (Outputs the reversed value of Index 41h bit 0.)
AUDIO	O	Not affected by SLEEP# pin. (Outputs the reversed value of BVD2/SPKR# when Index 40h bit 0 is 1, and LOW otherwise.)
IRQ	O	Not affected by SLEEP# pin.
PCIRQ	O	Not affected by SLEEP# pin.

B : Bidirectional
I : Input
O : Output

- PC card side

Pin name	I/O	State
CMEMRD#	O	High
CMEMWR#	O	High
CIORD#	O	High
CIOWR#	O	High
CD[15:0]	B	The state when SLEEP# pin goes to LOW is maintained.
CA[25:0]	O	The state when SLEEP# pin goes to LOW is maintained.
REG#	O	The state when SLEEP# pin goes to LOW is maintained.
CE1#, CE2#	O	The state when SLEEP# pin goes to LOW is maintained.
CRESET	O	Not affected by SLEEP# pin. (Outputs the value of Index 41h bit 4.)

B : Bidirectional
I : Input
O : Output

② Standby mode (Card side shut-down)

When either Index 41h bit 3 or bit 0 is 0, the J6951S goes into the standby mode and the card side signals are in the shut down state.
In the shut down state, the outputs (CA[25:0], REG#, etc.) to the J6951S are HI-Z state.
CD as well as the other output pins is driven to Hi-Z state when shut-down. In shut-down, no through current flows through the input I/O PAD of CD [15:0] even though the value at the pin is 0, 1 or an intermediate value. This eliminates unnecessary current consumption in shut down state. The input signal value is fixed to LOW inside the J6951S.
The inputs (BVD1, CWAIT#, etc.) from the J6951S except for CD1# and CD2# are fixed to HIGH inside the J6951S regardless of the input signal values. To these input signals, the through current protection is not applied. These input signals must be pulled up in the system side according to the JEIDA Ver. 4.1 regulations.
CD1# and CD2# normally operate under the shut-down state. (CD1# and CD2# have no shut down state.)
The states of pins under the shut down state are shown below.
"Have no shut down state" means the pins operate normally whether they are under the shut down state or not.

- CPU side

Pin name	I/O	State
SD[15:0]	B	Has no shut down state. (Since, however, CD[15:0] input is fixed to LOW inside the J6951S, when it is tried to read the PC card, data with all bits at LOW are read.)
SA[20:0]	I	Has no shut down state.
IRQ	O	Has no shut down state.
PCIRQ	O	LOW (This has no shut down state. Since, however, RDY/BUSY# and IRQ# are fixed to LOW inside the J6951S, though Index 42 bit 1 is 1 in the I/O card mode, it cannot be HIGH. Therefore, always LOW.)
SLEEP#	I	Has no shut down state.
RESET#	I	Has no shut down state.
BHE#	I	Has no shut down state.
CLK	I	Has no shut down state.
MREQ#	I	Has no shut down state.
IOREQ#	I	Has no shut down state.
RD#	I	Has no shut down state.
CS16	O	Has no shut down state. (Since, however, WP/IOIS16# is fixed to HIGH inside the J6951S, when an access is tried to the PC card with Index 44h bit 2=0 in the I/O card mode, CS16 is drive to LOW.)
WAIT	O	Has no shut down state. (Since, however, CWAIT# is fixed to HIGH inside the J6951S, only LOW output can be issued.)
AUDIO	O	LOW (Has no shut down state. Since, however, BVD2/SPKR# is fixed to HIGH inside the J6951S, only LOW output can be issued.)
CPON#	O	Has no shut down state.

B : Bidirectional
I : Input
O : Output

- PC card side

Pin name	I/O	State
CD[15:0]	B	Hi-Z
CA[25:0]	O	Hi-Z
CMEMRD#	O	Hi-Z
CMEMWR#	O	Hi-Z
REG#	O	Hi-Z
CRESET	O	Hi-Z
CIORD#	O	Hi-Z
CIOWR#	O	Hi-Z
CE1#, CE2#	O	Hi-Z
CD1#, CD2#	I	Has no shut down state.
BVD1	I	Fixed to HIGH inside the J6951S.
BVD2/SPKR#	I	Fixed to HIGH inside the J6951S.
WP/IOIS16#	I	Fixed to HIGH inside the J6951S.
RDY/BUSY#, IRQ#	I	Fixed to HIGH inside the J6951S.
CWAIT#	I	Fixed to HIGH inside the J6951S.

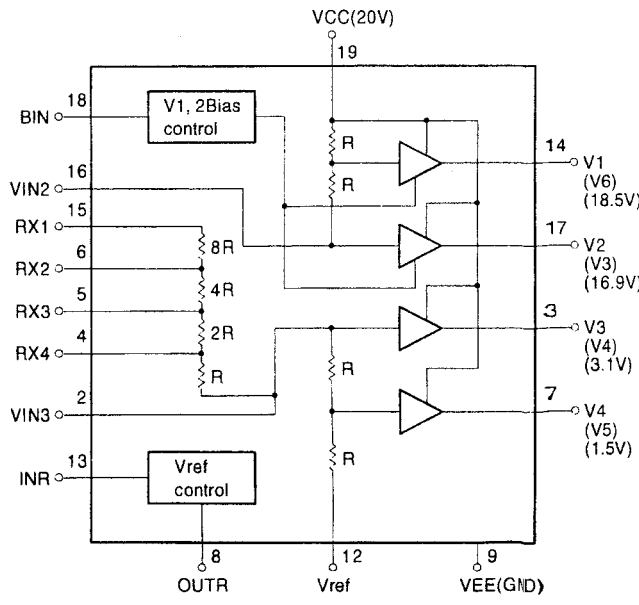
B : Bidirectional
I : Input
O : Output

3-4. LVC (LA5318V)

1) General descriptions

This IC controls the liquid crystal drive power source.
This IC divides a voltage generated externally (about 20V at normal temperature Ta: 25°C) into 1/13 bias and outputs at V1 - V4.

2) Block diagram

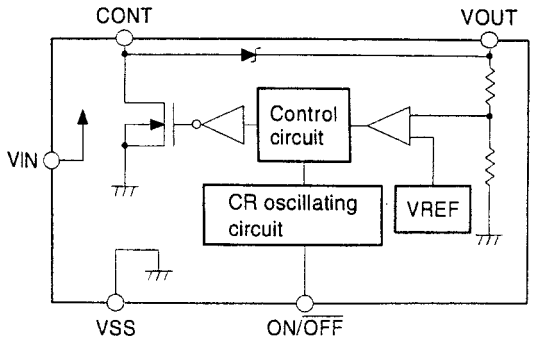


* Signal names in ( ) show signals for the circuit.

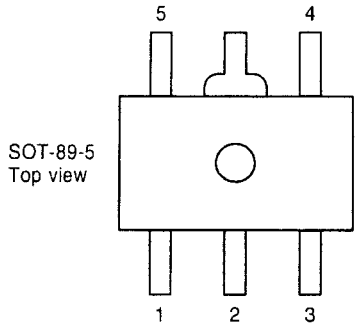
3-5. Booster IC (S-8435FF)

The S-8435F for boosting the voltage from 5 V to 12 V.

1) Block diagram



2) Pin layout

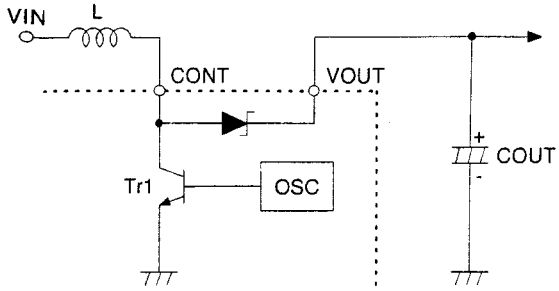


Terminal	S-8435	Description
1	CONT	CONT: External inductor connection terminal
2	V_{SS}	GND terminal
3	ON/$\overline{OFF}$	Power-off terminal H: Normal (step-up) operation L: Step-up off (Oscillating circuit off)
4	V_{IN}	Positive power supply terminal
5	V_{OUT}	Output voltage terminal

3) Operational description

The S-8435 booster IC is composed of a power Tr1, a crystal oscillator circuit, a Schottky diode, etc.

Tr1 is turned on and off by the crystal oscillator circuit. While Tr1 is on (t_{ON}), energy is accumulated in the inductor (L) and when Tr1 is turned off (t_{OFF}), accumulated energy is supplied through the diode to the capacitor (C_{OUT}) connected to V_{OUT}.



Crystal oscillator circuit: Oscillator composed of a capacitor and a resistor. Its oscillation frequency is 30 kHz typ.

ON/$\overline{OFF}$ terminal: This terminal is intended to stop or start the boosting operation. If this terminal is set to the "L" level, all of the internal circuits stop, reducing current consumption greatly. A voltage between VSS 0.3 V and VSS 13 V can be applied to this terminal irrespective of the input voltage.

Power-off terminal	Crystal oscillator circuit	Output voltage	Current consumption	
"H"	On	Fixed	15 µA typ.	
"L"	Off	≃ V_{IN}*	0.2 µA max.	S-8435: CONT = HI-Z

* This voltage can be obtained by subtracting a voltage drop due to the dc resistance of the inductor and the forward voltage of the diode from V_{IN}.

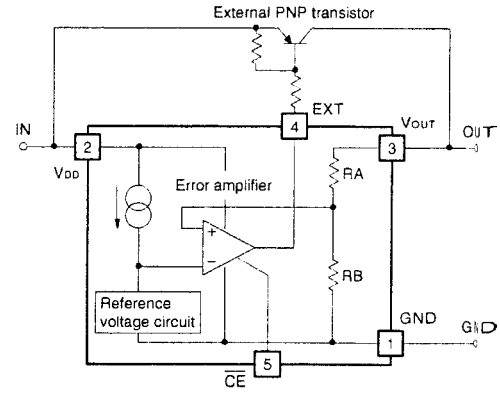
Schottky diode: This diode has almost the same characteristics as the small signal diode 1S1588.

3-6. Voltage regulator (RN5RG50) (RN5RG37)

This IC is the positive voltage regulator with external transistors, and is composed of the reference voltage power, the error amplifier, the output setting resistor network, etc.

The output voltage Vout is detected with feedback resistors RA and RB, and compared with the reference voltage in the error amplifier. In this manner, the base current of external PNP transistor is adjusted to keep the output voltage Vout at a constant level.

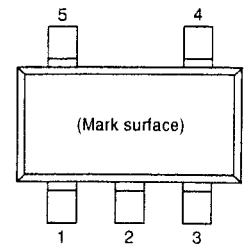
1) Block diagram (including the external circuit)



2) Pin descriptions

Pin No.	Name	Function
1	GND	GND pin
2	V_{DD}	Input pin
3	V_{OUT}	Output pin
4	EXT	External transistor drive pin (Nch open drain output)
5	$\overline{CE}$	Chip enable pin

3) Pin arrangement



3-7. Flash Memory (MBM29F040A-12)

1) General Description

The MBM29F040A-12 Flash Memory, with 4,194,304-bit capacity and a single 5-volt power supply, offers capabilities for both batch erasure of the entire chip and erasure by sector unit, and for byte programming.

The memory cells utilize a stack-gate transistor, which is used in a conventional EPROM. The CMOS design of the peripheral circuit allows high-speed operation with significantly reduced power consumption in both operating and stand-by modes.

With a 512K word (64K × 8 sector) × 8-bit configuration, the MBM29F040A-12 enables erasure of 64K sector blocks, meeting the JEDEC terminal array standard.

A 32-pin thin small output package (TSOP) is used.

A programming algorithm automatically verifies the generation of erase or program pulses inside the device after each erase or program command sequence is entered. Completion time is about 1.0 second for single-sector programming, and 1.5 seconds or less for single-sector erasure.

Electrical data can be erased and programmed through written commands to alter data within the system, making the MBM29F040A-12 Flash Memory an outstanding choice for a wide range of applications.

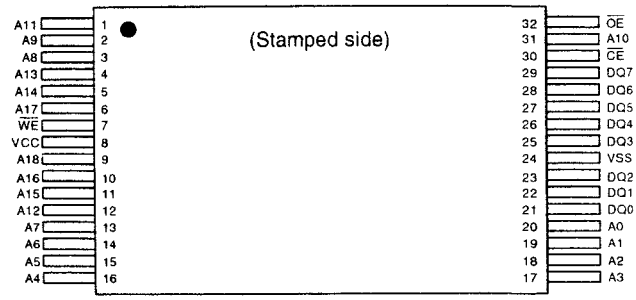
2) Characteristics

Characteristics		MBM29F040A-12
Access time (max.)		120 ns
Power supply voltage		5.0 V±10%
Power consumption (max.)	Read	220 mW
	Erase / Program	330 mW
	TTL standby	5.5 mW
	CMOS standby	0.55 mW

3) Features

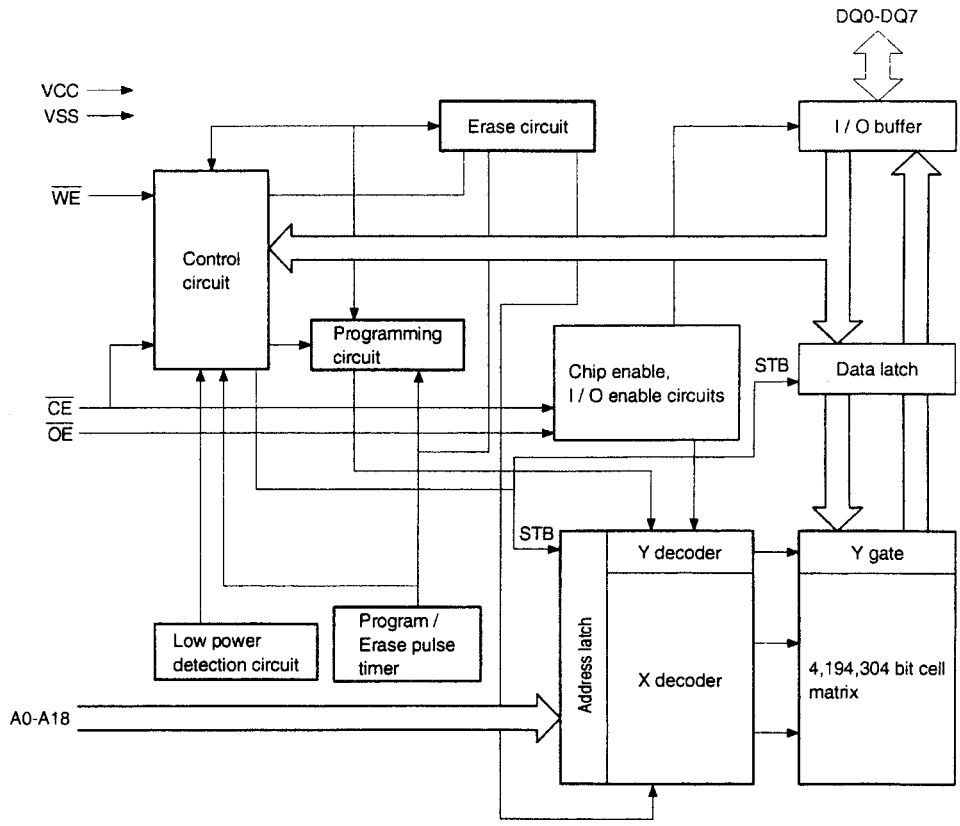
- 512K word (64K × 8 sectors) x 8 bit configuration
- Silicon-gate CMOS technology
- Stack-gate structure cell technology
- Single +5 V power supply for Program / Erase / Read
- Input / output TTL level
- Three-state output
- Automatic program algorithm (Embedded Algorithm)
- Automatic Erase / Program

4) Pin Arrangement



Symbol	Terminal
A0 ~ A18	Address input
DQ0 ~ DQ7	Data input / output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
Vss	Ground
Vcc	Power supply (+5.0 V ±10%or ±5%)

5) Block Diagram



3-8. Pseudo Static RAM (LH6P82T)

1. General description

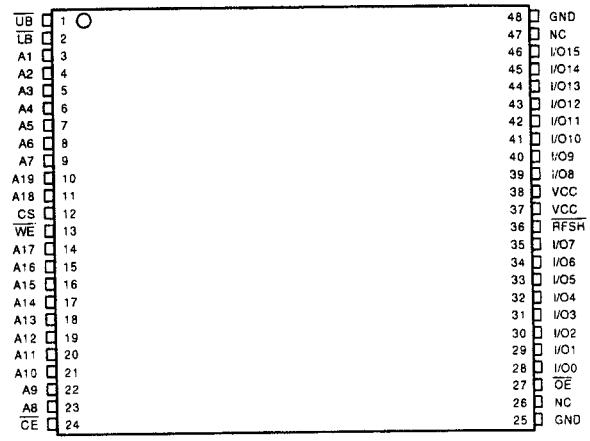
The LH6P82T Pseudo Static RAM has a 524,288 word × 16 bit configuration. It includes independent $\overline{RFSH}$ and $\overline{OE}$ terminals which can also be connected together to form an $\overline{OE}$ / $\overline{RFSH}$ terminal. Thus substitution is easily possible from a 4Mbit pseudo-static ram.

2. Characteristics

- Configuration 524,288 word × 16 bit
- $\overline{CE}$ access time 120 ns (max.)
- Minimum cycle time 190 ns (max.)
- Power consumption
  - Operating mode 150 mW (max.)
  - Standby mode 360 µW (max.)
  - Data hold mode 300 µW (max.)
- Full I/O LVTTL compatibility
- Auto-refresh possible via $\overline{RFSH}$ terminal
- Self-refresh possible via built-in oscillator
- 4096 refresh cycle (64 ms)
- Non-multiplex address
- Byte access possible via $\overline{UB}$ and $\overline{LB}$ terminals
- Power supply voltage 3.0 ~ 3.6 V
- Package: 48-pin TSOP Type I (TSOP048-P-1218)
- Non-radiation-resistant design
- Plastic package
- P type silicon substrate
- CMOS process (structural)
- Operable temperature range 0 ~ 70°C (32 ~ 154°F)

3. Terminal Names and Layout

48-pin TSOP type I (TSOP048-P-1218)



Top View

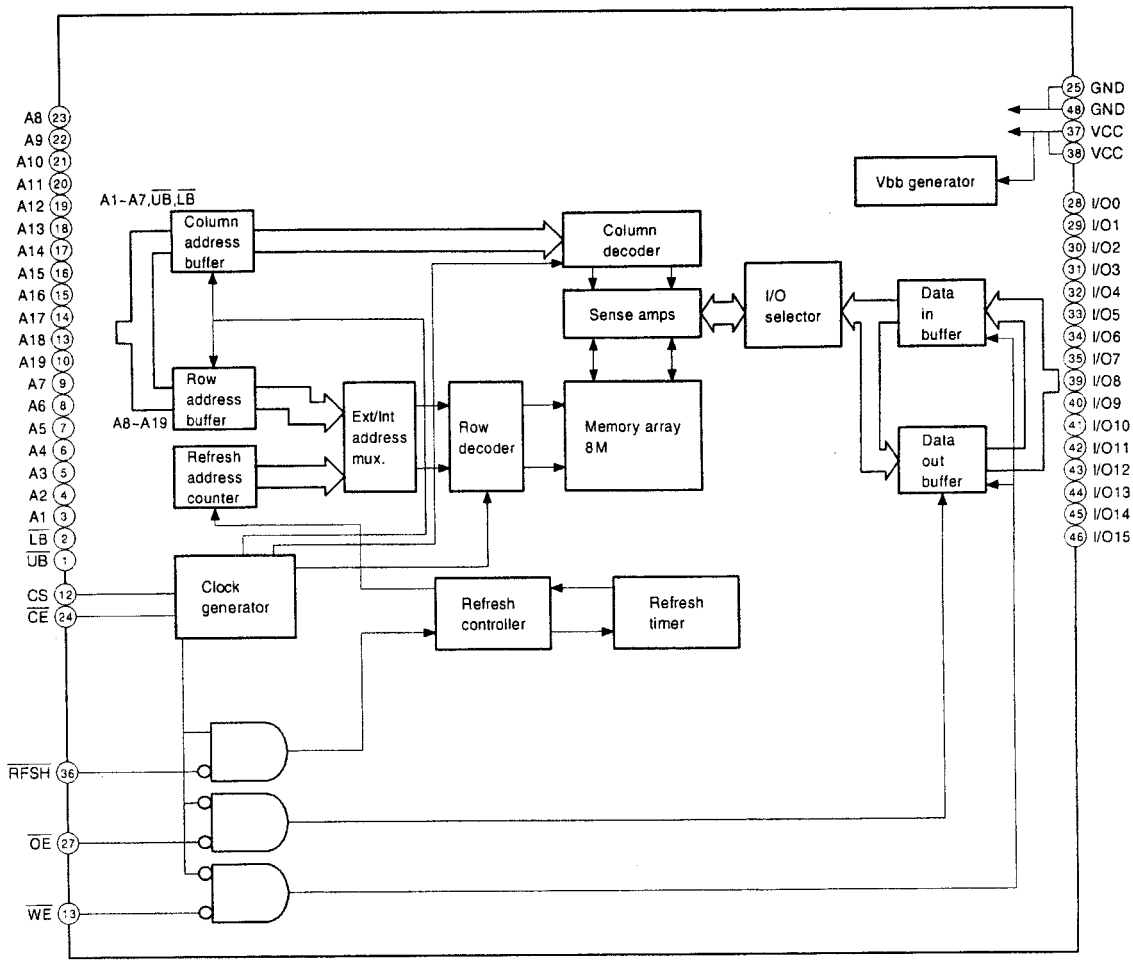
Symbol	Terminal
A_8 ~ A_{19}	Row address input
A_1 ~ A_7	Column address input
$\overline{UB}$, $\overline{LB}$	Superior / inferior byte enable input
$\overline{RFSH}$	Refresh input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
$\overline{CE}$	Chip enable input
CS	Chip select input
I/O_8 ~ I/O_{15}	Superior byte data input / output
I/O_0 ~ I/O_7	Inferior byte data input / output
V_{CC}	Power
GND	Ground

$\overline{CE}$	CS	$\overline{RFSH}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	Mode		I/O 0 ~ 7	I/O 8 ~ 15
L	H	X Note 1	H	L	H	L	Read	Inferior byte access	Output data	High-Z
					L	H		Superior byte access	High-Z	Output data
					L	L		Word access	Output data	Output data
					H	H		Invalid	High-Z	High-Z
L	H	X Note 1	L	X	H	L	Write	Inferior byte access	Input data	High-Z
					L	H		Superior byte access	High-Z	Input data
					L	L		Word access	Input data	Input data
					H	H		Invalid	High-Z	High-Z
H	X	L	X	X	X	X	Auto-refresh		High-Z	High-Z
L	L	H	X	H	X	X	CS standby		High-Z	High-Z
H	X	H	X	X	X	X	Standby		High-Z	High-Z

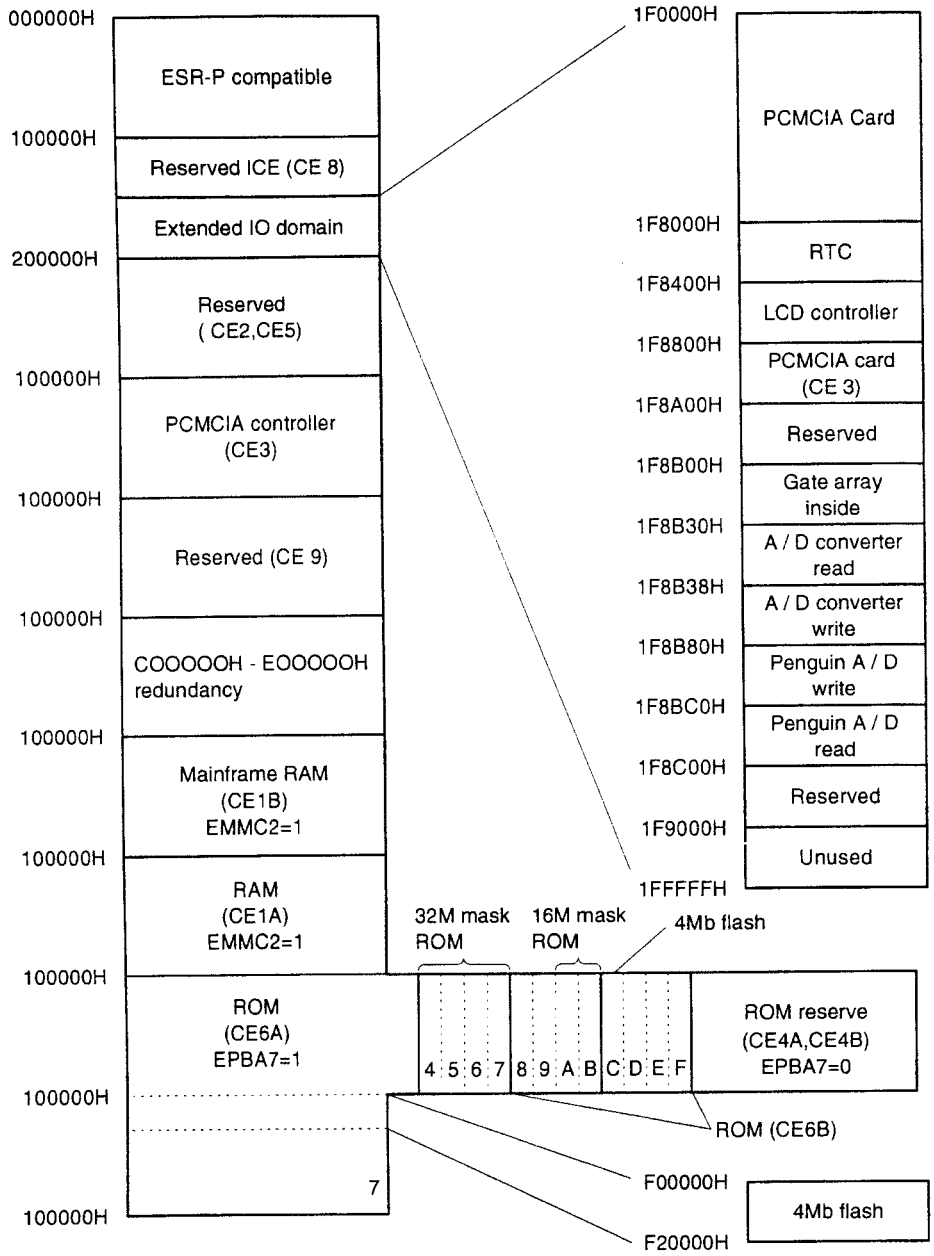
H = High, L = Low, X = Don't Care

Note 1: When $\overline{RFSH}$ = L, $\overline{RFSH}$ fall time must satisfy t_{RDH}

4. Block Diagram



4. Memory I / O Map



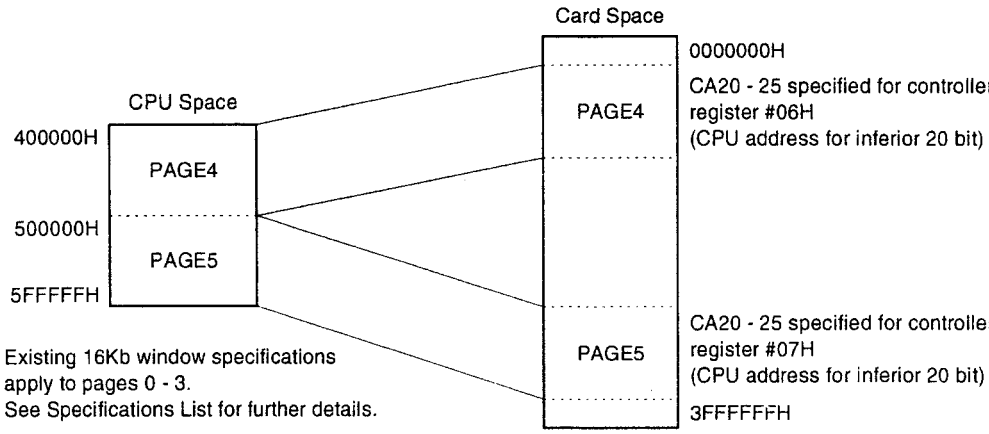
NOTES: 1) RAM available in 8Mbit × 1 and 8Mbit × 2 versions.
2) Connection of 16Mbit ROM to CE6A and 32Mbit ROM to CE6B allows either EEPROM or flash ROM to be connected to the CE6B bank.

Appendix to Memory Map

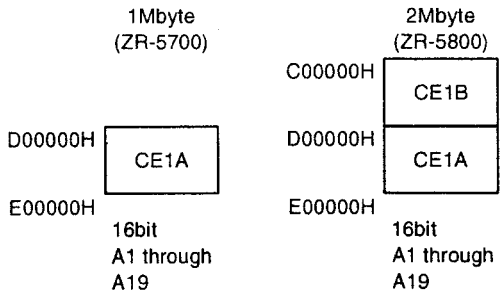
1. PCMCIA Memory

The memory utilizes the 2Mb 400000H ~ 5FFFFFH space in the CPU, with no bank function built into the CPU. It is therefore necessary to set ECBNK (4026H) = 01H before using.

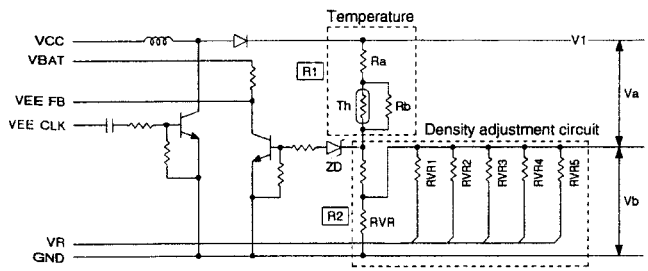
Controller As illustrated below, viewed from the CPU, 64Mb is allocated by window function in 2Mb spaces. Under this arrangement, two windows of 1Mb may be used (2Mb series also possible.)



2. RAM



5. LCD contrast adjustment and temperature correction circuit



① Contrast adjustment circuit

The contrast adjustment is performed by the electronic VR as follows: Data is latched from the CPU to the common Dri, which outputs the latched data (5 bit, VR1 ~ VR5) to adjust the LCD power V1.

In the above figure, suppose that the combined resistor in the temperature correction circuit is R1 and the combined resistance in the density adjustment circuit is R2, the relationship between Va/Vb and R1/R2 is as follows:

- Va : Vb = R1 : R2

$$Va = \frac{Vb \times R1}{R2}$$

- Vb is maintained at constant by zenor diode (ZD).
- R1 is a fixed resistance.
- Therefore, Va decreases as R2 increases. (In inverse proportion.)

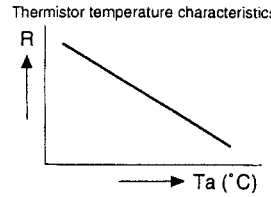
As a result, V1 can be adjusted by adjusting R2.

R2 value is parallel combined value of RVR ~ RVR5 with the output data (VR1 ~ VR5) from the common Dri, and can be adjusted in 32 steps by the output data.

② Temperature correction circuit

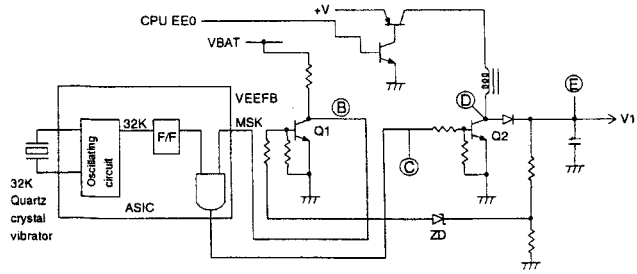
Temperature correction is performed, contrary to the above, by changing the ambient temperature to adjust the R1 value.

R1 is composed of the combined resistance of Ra and Rb/Th. Since Th (Thermistor) has characteristics of varying resistance by temperature, the combined resistance R1 varies according to the ambient temperature. As the temperature decreases, the thermistor resistance increases, therefore R1 also increases. As a result, Va is increased to increase V1.



6. LCD boost circuit

The power voltage to drive the LCD is generated by the step-up type, chopper system convertor. The operating principle is described below:

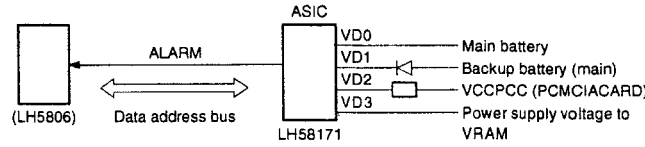


Clock of about 32KHz is supplied from ASIC. Supply/stop control of the clock to the convertor is allowed with DF/F output of GA. When the machine is ON, Ⓕ is driven to HIGH, supplying the clock to the convertor. When the machine is OFF, Ⓕ is driven to LOW, keeping point Ⓐ at LOW.
The operating principle is: clock is supplied to point Ⓐ. When point Ⓑ is also HIGH, Q2 is turned on/off by IC1 output. During Q2 ON, energy is charged in coil L. During Q2 OFF, energy is discharged from coil L. The output voltage is controlled by zenor diode ZD. When the output exceeds the zenor voltage plus Q1 VBE, Q1 is turned on. Point Ⓑ is driven to LOW, and point Ⓒ is fixed to LOW until the output voltage falls, stopping the convertor.
The waveform of each section is shown below. (The negative feed-back is performed so that V1 is kept at constant.)
Start/stop of the boost circuit is performed by EE0 of the CPU. When the unit is OFF, no voltage is applied to V1.

7. Low battery detection

The main battery level is monitored in two stages. When a low battery is sensed first, the BATT. indicator is turned on (caution level). If a further drop is found, it turns off (fatal level).
It also monitors the backup battery and the RAM card data protection battery voltage.

- Operation theory



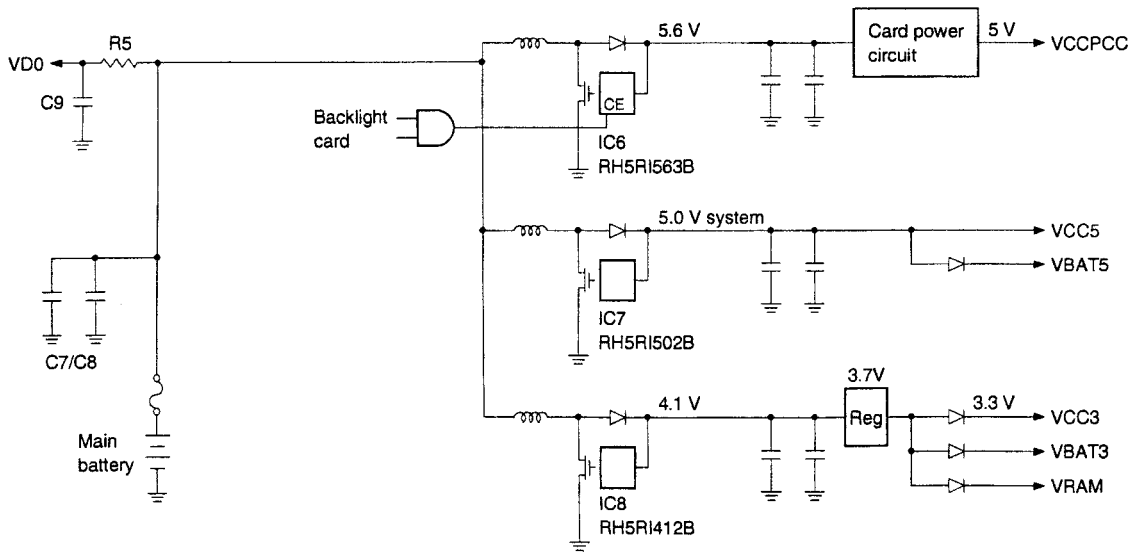
The low battery function is incorporated in ASIC (LH58171), the detection level and the detection line are switched by software. When a low battery is found by ASIC, a high state of signal is issued onto the ALARMS line to inform the occurrence to the CPU.

① Main battery detection
Software switch is done using the VD0 line of ASIC to select a two-stage detect level. The input is at 1.5 ~ 2.5V when the caution level is discovered.

② Backup battery detection
The internal switch is selected on VD1 and VD2, VD3 lines of ASIC, and a single internal detector is used to detect.

8. Power Circuits ZR5700 / 5800

These power circuits are broken down into 5 V, 3.3 V, and 5.6 V systems. The 5V and 3.3 V systems are always on during operation. The ZR5700 5.6 V system comes on only when a card is used. The ZR5800 5.6 V system comes on only when the backlight is illuminated.



Vcc5: 5 V system without backup CPU, 32M masked ROM, 16M masked ROM, 4M flash, PCMCIA controller

Vbat5: 5 V system with backup ASIC

Vcc3: 3.3 V system without backup CPU, PCMCIA controller, VRAM, LCD Dri.

Vbat3: 3.3 V system with backup ASIC

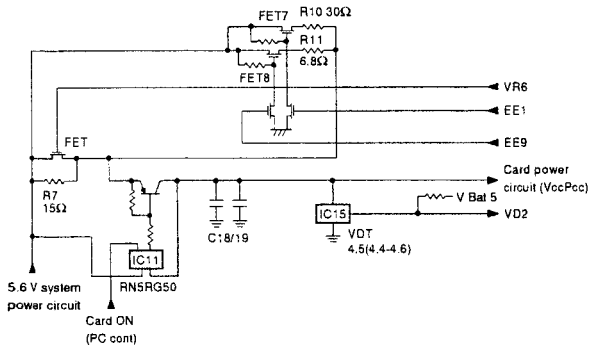
VRAM: 3.3 V system with backup 8Mb RAM

VccPcc: 5 V system without PCMCIA card, PCMCIA controller card side power supply

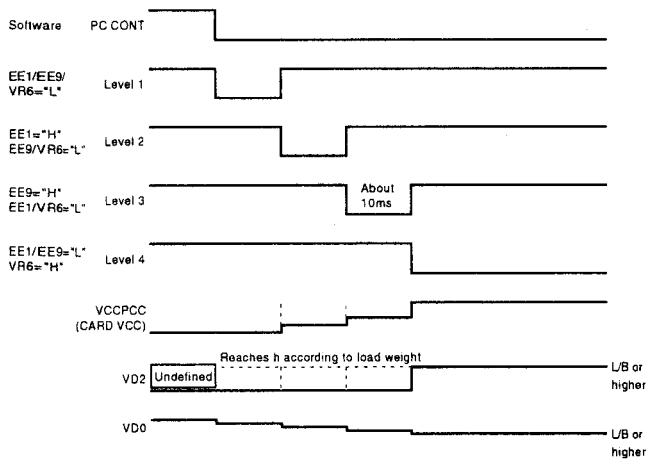
Each power circuit includes a DC-DC converter IC, and is available with various voltages.

9. Card Power Circuit

The card power circuit has been enhanced to enable use of a high-speed modem card even when operating only with the main battery.
To reduce the effect of card use on the system-side power circuit, a phased electric current supply is utilized to increase capacity when the card is inserted and the power is turned on.
A separate DC-DC converter for card use is provided for the system-side power circuit.
Phasing of the current supply for increased capacity is in four levels, controlled by three signals in the software. (See Attachment 1)
During the phased increase of power suppply capacity, the main battery L/B of the main unit and the voltage of the card power circuit are monitored by the VD0 and VD2 terminals, respectively, of the ASIC. If the main battery and card power supply voltages are insufficient, cut off the card power circuit and use the software for control.



Attachment 1



10. Step-down DC-DC Controller (MAX1651CSA)

1) Outline

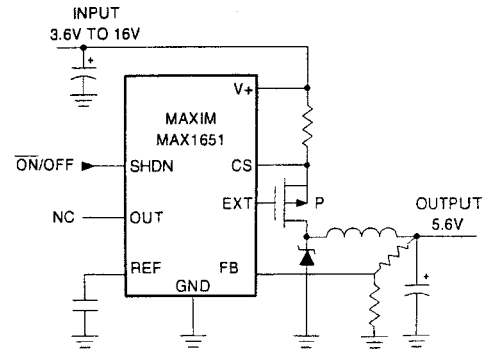
MAX1651CSA is a BICMOS step-down DC-DC controller which has realized a high efficiency in the load current range as wide as 1 mA ~ 2.5 A. The pulse frequency modulation (PFM) control system by unique current limitation provides it with both the advantages of high efficiency at heavy load application in pulse width modulation (PWM) and current consumption as low as 100 µA (2 mA ~ 0 mA in PWM). It is also very excellent in dropout characteristics (300 mV) owing to high switch duty cycle (96.5%) as well as low current detection threshold (110 mV). The high switching frequency (~ 300 kHz) enables the operation with small external parts attached to it.
MAX1651CSA is provided with a dropout voltage of lower than 0.3 V at 500 mA output and allows an input voltage of up to 16 V. The output voltage is internally set at 3.3 V. Besides, if two resistances are used, the output voltage can be set freely between 1.5 V and the input voltage.

This step-down controller can drive the external P-channel MOSFET transistor and supply power of higher than 12.5 W. If the power needed is smaller, use any of the MAX639/MAX640/MAX653 step-down controllers which are equipped with FET and capable of supplying load current of up to 225 mA.

Application

- PDA
- High efficiency step-down regulator
- Green PC for reduction from 5 V to 3.3 V
- Battery driving equipment

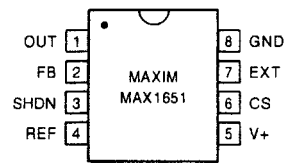
Operating Circuit



2) Features

- High efficiency of more than 90% (10 mA ~ 1.5 A load)
- Output power of more than 1.25 W
- Drop-out voltage: 0.3 V (at load of 500 mA)
- Self current consumption: 10 µA max.
- Shutdown current: 5 µA max.
- Max. input voltage: 16 V
- Control system by current limitation
- Switching frequency up to 300 kHz
- Duty cycle: 96.5%

3)Pin Locations



4)Terminals

No.	Name	Function
1	OUT	Detecting input for working 5 V or 3.3 V fixed output. This terminal is connected internally to voltage divider. This is to be connected to output terminal of the circuit but does not output radio wave. Do not connect this terminal in variable output operation. This is kept open in this controller.
2	FB	Feedback input. Connect this terminal to GND in fixed output voltage operation. In variable output voltage operation, connect a resistance type voltage divider between OUT, FB and GND terminals. See "Setting Output Voltage".
3	SHDN	Shutdown input for active "High". Output is shut down in "High". In shutdown mode, REF, OUT and external MOSFET are turned Off. Connect this terminal to GND for normal operation.
4	REF	1.5 V reference output, which has 100 μA current source capacity. Bypass this terminal with 0.1 μF capacitor.
5	V+	Positive power source voltage input
6	CS	Current detecting input. Connect current detecting resistance between V+ and CS. External MOSFET is turned OFF when voltage of this detecting resistance becomes equal to current limitation trip level.
7	EXT	Terminal for driving external P-channel MOSFET gate. EXT swings by voltage generated between V+ and GND.
8	GND	Ground

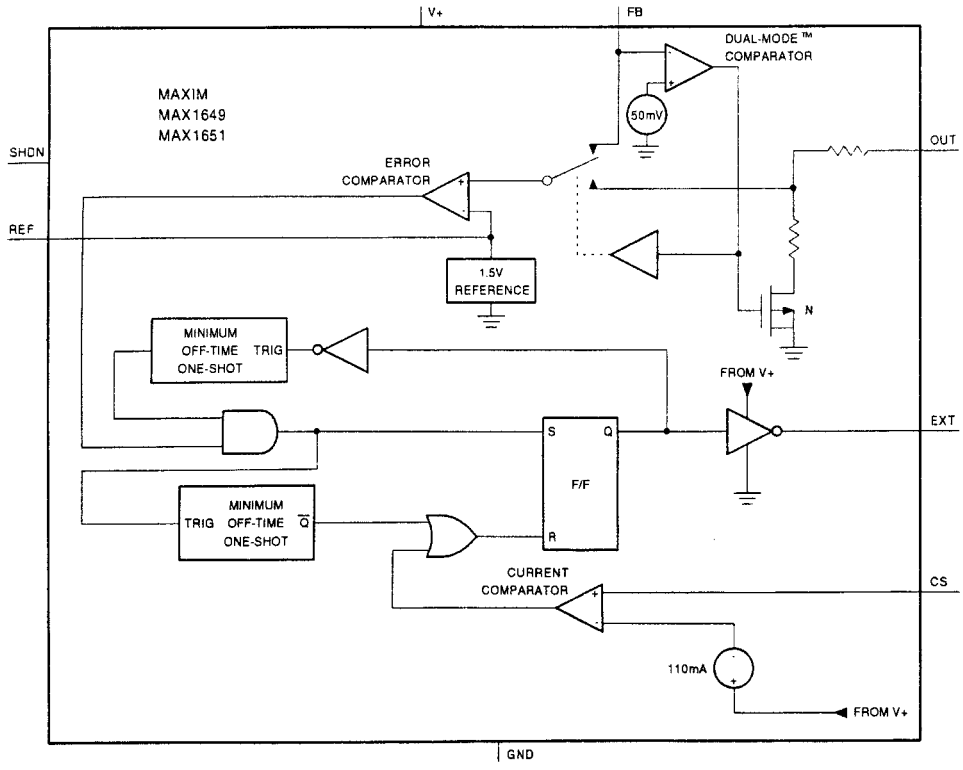
5)Explanation

MAX1651CSA is a BiCMOS stepdown switch mode power controller and supplies fixed output voltages of 3.3 V. The unique control system combines the advantages in pulse frequency modulation (low current consumption) and pulse width modulation (high efficiency at heavy load application). The external P-channel power MOSFET makes it possible to increase the peak current over 3 A and the output current capacity substantially as compared to the conventional PFM products. Fig. 2 shows the block diagram.
MAX1651CSA has the following four improved points as compared to the conventional products:

1) The converter is operated by a small surface-mounted inductor at 300 kHz switching frequency.
2) The current limiting PFM control system realizes more than 90% high efficiency at a wide range of load current (10 mA ~ 1.5 A).
3) Drop-out voltage is reduced down below 300 mW.
4) Maximum self current consumption is as low as below 100 μA.

Pulse Frequency Modulation Control System

MAX1651CSA adopts an unique PFM control system by current limitation. Like ordinary PFM converters, the external power MOSFET is turned ON when the voltage converter detects an output voltage drop. However, unlike ordinary PFM converters, the switching is controlled by the combination of a pair of one-shots which set the current limit and the maximum switch-ON time (32 μs) and minimum switch-OFF time (1.1 μs). Once turned OFF, the switch is held OFF for 1.1 μsec. by one-shot of OFF time. After the minimum Off time elapses, the switch is: 1) turned OFF when the output is being stabilized; or 2) turned ON again if the output is lower. MAX1651CSA can be operated in continuous conduction mode by limiting the peak current and maintains a high efficiency even at heavy load application (Fig. 3). The current limiting function is one of the major characteristics in the control circuit. Once turned ON, the switch is held ON until: 1) the one-shot of the maximum ON time is turned OFF (after 32 μs) or; 2) the maximum current limit is reached.
EXT swings at the voltage between V+ and GND and outputs the driving force to the external P-channel power MOSFET transistor.



™ Dual-Mode is a trademark of Maxim integrated Products

Shutdown Mode

The nominal self current consumption of the device in normal operation is 78 µA. But in actual circuit, the current running through the external feedback resistance (if used) and leak current of diodes and capacitors are added to it. In the circuit diagram of Fig. 1, the power consumption of the entire circuitry becomes 90 mA when V+ is 5 V and the output voltage 3.3 V.

Operation Mode

At the time of high output current supply, MAX1651CSA work in continuous conduction mode. In this mode, current runs at all times through the inductor and the control circuit maintains regulation within a range not exceeding the current supply capacity of the switch while controlling the duty cycle of the switch (Fig. 3). This offers an excellent load transit response and high efficiency.

In intermittent conduction mode, the inductor starts its current level from zero, increases it to the peak and lowers to zero. Despite of its excellent efficiency in this mode, output ripples are generated some more frequently and ringing may be generated in the switching waveform (due to self-resonant frequency of inductor). This ringing is nothing more than likely one which does not affect the operation at all.

Drop-out

MAX1651CSA enters into drop-out state when the input voltage (V+) lowers and the output drops below the minimum output voltage rating (see the electrical characteristics). The drop-out voltage indicates a voltage difference between the input and output in this state. As for the relationship between the drop-out voltage and the temperature, refer to the standard operation characteristics graph.

Output Voltage Setting

The output voltage of MAX1651CSA is set at 3.3 V, with FB connected to GND for fixed output operation. The output voltage can also be varied within a range of 1.5 V ~ input voltage with use of external resistances R2 and R3 as shown in Fig. 4. The resistance value 150 kΩ is an appropriate value well capable of preventing excess power consumption as well as RC delay caused by parasitic capacity of FB pin. The resistance value of R2 is obtained by the following formula:

$$R2 = R3 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

where, V_{REF} = 1.5 V

When using external resistances, OUT may be either connected to the output or kept open.

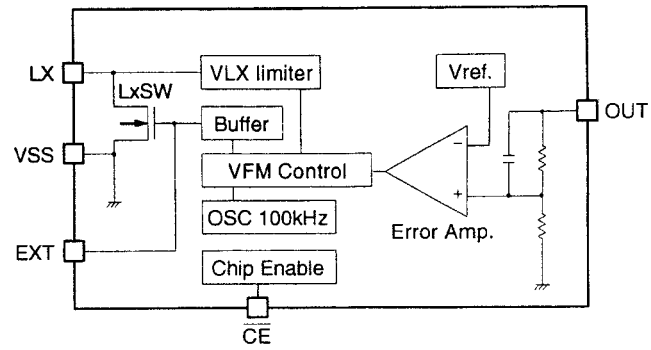
(In MAX1651CSA, the output voltage is set at about 5.6 V.)

Selection of Current Detecting Resistance

The current detecting resistance limits the peak switch current to 110 mV/RSENSE. RSENSE represents the current detecting resistance value, and 110 mV the current limiting trip level (see electrical characteristics).

11. Step-up DC/DC Converter (RH5RI412B, 502B, 563B)

1) Circuit block diagram

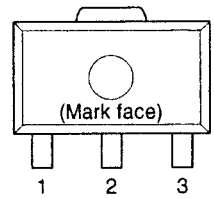


Note: Lx terminal ..... for 563B only
CE terminal .... for 563B only

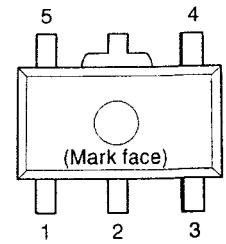
2) Terminals

Terminal No.		Name	Function
XX2B	XX3B		
1	5	Vss	Ground
2	2	OUT	Step-up output voltage monitoring, IC internal power supply
—	4	Lx	Switching terminal (Opened lane)
3	3	EXT	External Transistor drive terminal (CMOS output)
—	1	CE	Chip enable terminal (Active "Low")

3) Terminal configuration



xx2B type

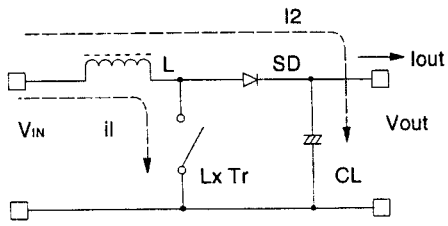


xx3B type

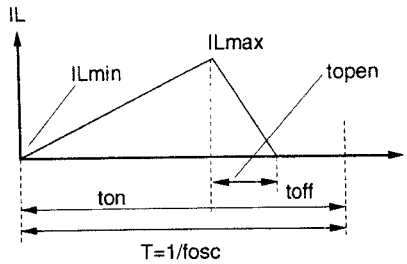
4) Operation of step-up DC/DC converter and output current

The step-up DC/DC converter steps up the output voltage higher than the input voltage by means of the Lx transistor turning ON to release this energy together with input power. The explanation will be given stepwise according to the figure below:

<Basic Circuit Diagram>



<Current running through L>



Step 1: Lx Tr turns ON, current IL = i1 runs and energy is charged to L. At this moment, current IL = i1 increases from Ilmin. = 0 in proportion to the time (ton) during which Lx Tr is ON and reaches IL max.

Step 2: Since L keeps IL to be maximum when Lx Tr turns Off, shot key diode (SD) is turned ON to run current IL = i2.

Step 3: IL = i2 decreases gradually and it becomes IL = Ilmin. = 0 after "topen" time elapses to turn OFF SD.

In VFM control system, the output voltage is kept constant by fixing "ton" and controlling step-up frequency (fosc) per unit time.
When the set-up action is stable in a fixed state, the maximum current value (Ilmax.) and minimum current value (Ilmin.) running through the coil become same at either time when Lx Tr is ON or Off, as shown in the figure above.
In VFM system, duration of "toff" is normally longer than that of "topen" as shown in the figure above. In this case, energy accumulated in the coil for the time "ton" is all released for the time "toff" and Ilmin. becomes zero.

12. EL Panel driver

1) Ordering Information

Device	Package Options
	8-Lead SO
HV801	HV801LG

2) Features

- Processed with HVCMOS® technology
- 4.5V to 10V supply voltage
- DC to AC conversion
- Programmable output current
- Output short circuit protection
- Wide output load range from 0 to 21nF
- Adjustable output lamp frequency

3) Application

- Portable instruments
- Clocks
- Apparels

4) Absolute Maximum Ratings

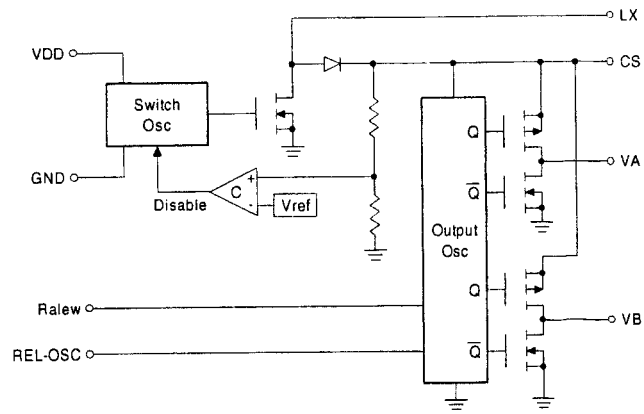
Supply Voltage, V_{DD}[1]	–0.5V to +11V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

Note:
1. All voltages are referenced to GND.

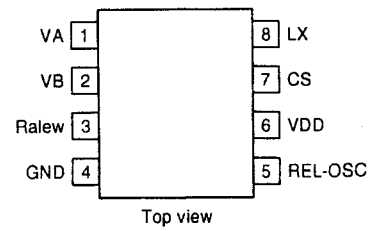
5) General Description

The Supertex HV801 is a high-voltage driver designed for driving EL lamps of up to 21nF. The input supply voltage range is from 4.5V to 10V. The device uses a single inductor and a minimum number of passive components. The maximum output voltage that can be applied to the EL lamp is ±110V. The output current can be programmed by connecting an external resistor between R_{slew} and V_{DD}. As the value of R_{slew} decreases, the slew rate of V_A and V_B increases.
The HV801 has two internal oscillators, a switching MOSFET, and a high-voltage EL lamp driver. The frequency for the switching MOSFET is fixed internally. The EL lamp driver frequency is set by an external resistor connected between $R_{EL\text{-}osc}$ pin and the V_{DD} pin. An external inductor is connected between the Lx and V_{DD} pins. A 0.1 µF storage capacitor is connected between C_S and ground. The EL lamp is connected between V_A and V_B.
The switching MOSFET charges the external inductor and discharges it into the 0.1µF capacitor at C_S. The voltage at C_S will start to increase. Once the voltage at C_S reaches a nominal value of 90V, the switching MOSFET is turned off to conserve power. The outputs V_A and V_B are configured as an H bridge and are switching in opposite states to achieve 180V peak-to-peak across the EL lamp.

6) Block Diagram

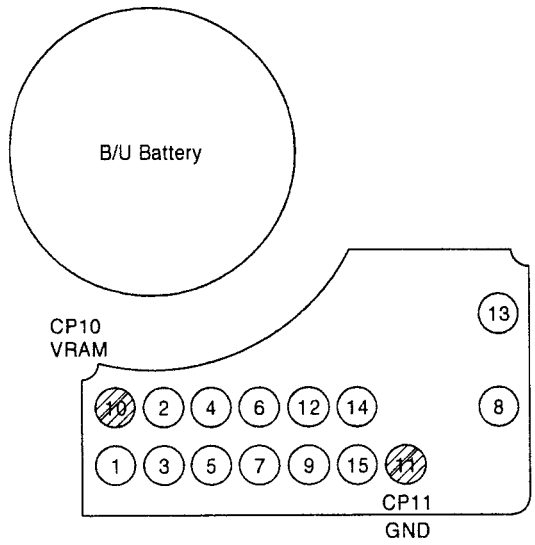


7) Pin Configuration



Top view
8-Pin DIP/SO-8

13. Servicing circuit



B/U Battery Compartment

(Check pad)

① F-OUT (ASIC)
② BTCOV (ASIC)
③ MAIN battery +3V
④ B/U +3V
⑤ VCCPCC (PCMCIA CARD)
⑥ VD3
⑦ VCC5
⑧ VCC3
⑨ $V_{Bat}5$
⑩ VPSRAM
⑪ GND
⑫ $V_{Bat}3$
⑬ V4.1
⑭ V5.6
⑮ VCCPCG (PCMCIA G/A)

14. Current consumption check

① OFF current measurement (main body)
Current consumption under OFF state must be max.
ZR-5700: 500μA
ZR-5800: 800μA

② Current measurement during display (main body)
The current consumption during display must be max. 24mA
("The earth mark with clock" displayed)

③ Backup current measurement
The backup current consumption must be max.
ZR-5700: 150μA
ZR-5800: 250μA

Note: External power supply
(Connecting to the main battery at +3V)

15. Shipment setting circuit

This unit employs a PSRAM instead of a conventional SRAM for memory. The PSRAM allows to flow a standby current of 20 times as great as that flowing in an SRAM.
Similarly to the conventional models, the main battery is packed together with the unit and the backup battery is installed in the unit. The backup battery may be exhausted before arriving at the user. In order to prevent against this, power supply to the PSRAM is electrically halted in the shipment setting.

(Note) When servicing also, do not leave the backup battery without necessary treatment.

① Turn on the shipment setting circuit. (Supply power to the VRAM.)
When the user installs the main battery and presses the [ON] key (or presses the [ON] key + RESET), the shipment setting circuit turns on (power is supplied to the VRAM). This is performed with the software.

② Turn off the shipment setting circuit (cut power to the VRAM).
When diag "40 DISABLE BACKUP BATTERY" is selected, the following display is shown and the setting circuit is turned off by the software. (The power to VRAM is cut off.)

BACKUP BATTERY DISABLE
OK

- Setting circuit state check
- When the setting circuit is off (Power to VRAM is cut off.)
- When the voltage between check pad "VRAM" and "GND" is 0 ~ 0.5V, the setting circuit is off.
- When the setting circuit is on (Power to VRAM is supplied.)
- When the voltage between check pad "VRAM" and "GND" is 2.3V or above, the setting circuit is on.

Caution:
Since this unit employs the PSRAM (Pseudo-SRAM) as its memory, if it is left only with the backup battery, the backup battery will be exhausted soon. Therefore, the main battery must be installed. (Do not leave the unit only with the backup battery.) When installing the both batteries after removing them for repair, first install the backup battery then install the main battery and reset the battery replacement SW and check that the initialize screen is displayed.

When power to the VRAM is cut off, the RAM data will be erased. Be sure to save the necessary data of the RAM before making the setting.

When the shipment setting circuit is broken:
Though the backup battery is new and the VRAM voltage is supplied, if the following display (same as that for the exhausted backup battery) is given, the shipment setting circuit may have been broken. In this case, be careful not to remove the 2 pin power or the main battery for protection of the memory content.

Replace main memory back-up battery. Please read the operation manual for directions. OK

(Note) In the ZR-5700/5800, never make the following settings before shipment, which will fasten backup battery exhaustion.

[B] and [S] keys

[B] and [C] keys

CHAPTER 3. NOTE FOR SERVICING

Caution:

1. This unit employs a PSRAM instead of a conventional SRAM for memory. The PSRAM allows to flow a standby current of 20 times as great as that flowing in an SRAM.
   Similarly to the conventional models, the main battery is packed together with the unit and the backup battery is installed in the unit. The backup battery may be exhausted before arriving at the user. In order to prevent against this, power supply to the PSRAM is electrically halted in the shipment setting.

   (Note) **When servicing also, do not leave the backup battery without necessary treatment.**

2. Before executing disassembly, assembly, diagnostic, rewriting of the flash EEPROM, etc., be sure to save the user data. (Refer to "4. Data exchange.") After servicing, set the clock to the punctual time and return the set to the user. (The clock is initialized by servicing.)

1. Shipment setting

Shipment setting procedure (After the inspection, be sure to perform the following shipment setting).

When diag "40 DISABLE BACKUP BATTERY" is selected, the following display is shown and the setting circuit is turned off by the software. (The power to VRAM is cut off.)

BACKUP BATTERY DISABLE
OK

- Setting circuit state check
- When the setting circuit is off (Power to VRAM is cut off.)
- When the voltage between check pad "VRAM" and "GND" is 0 – 0.5V, the setting circuit is off.
- When the setting circuit is on (Power to VRAM is supplied.)
- When the voltage between check pad "VRAM" and "GND" is 2.3V or above, the setting circuit is on.

(Note) In the ZR-5700/5800, never make the following settings before shipment, which will fasten backup battery exhaustion.
[B] and [S] keys
[B] and [C] keys

2. Resetting the ZR-5700/5800

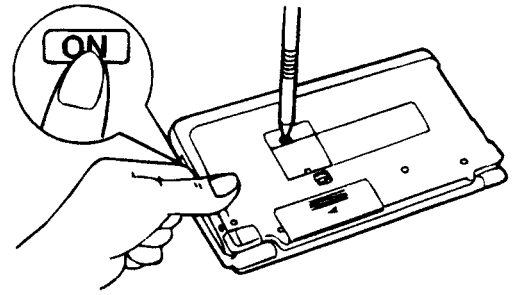
A strong impact, exposure to an electrical fields, or other unusual conditions may render the unit inoperative (Pressing keys and touching the display has not effect.). If this occurs, you must press the RESET switch on the back using the touch pen or similar object. Conditions that make the unit inoperative may also erase part or all of the data stored in memory.

- Do not use sharp objects or objects with breakable tips to press the RESET switch.

All reset operation

If the Organizer still fails to function after beening reset with the procedure above, or if you have forget the password to be entered at start-up, you must reset the unit using a more complicated procedure:

1. Hold down [ON] , while pressing and the RESET switch.



   A message appears.
2. Release [ON] .
3. Touch [NO] .
   The built-in clock and any set daily alarms will be reset.
   - Do not touch [YES] in step 3. (As this will delete all data in the unit.)
   - However, if you have forgotten the password for the start-up display, to use the unit you must touch [YES] , and lose all your data.

3. Battery Replacement

3-1. General guidelines

The unit uses the following types of batteries:

Use	Type	Size/Model	Qty.
Operation	Alkaline batteries	LR6 (AA)	2
Memory backup	Lithium battery	CR2032	1

There are some extremely important points to remember when installing new batteries:

- Do not remove the operating and backup batteries at the same time. Doing so will result in the loss of all data stored in the unit's memory.
- Backup all important data before replacing the batteries.
- Remove any installed PCMCIA card before replacing the batteries. If an IC card contains its own batteries, confirm that those batteries are not depleted before removing the card from the unit.
- Replace both operating batteries at the same time with new batteries of the same type.
- The memory backup battery installed at the factory. It drains slightly during shipment and distribution, so it may not achieve the lifetime indicated in the specifications.

Caution:

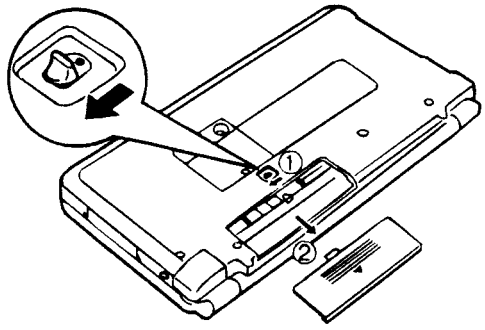
- Keep batteries out of the reach of children.
- If the unit will not be used for a long period of time, turn the unit on once a month and confirm that BATT doesn't appear at the top of the display (or replace the batteries beforehand). Leaving spent batteries in the unit may cause battery leakage and damage from corrosion.
- Do not dispose of batteries in a fire, they may explosions.

3-2. Replacing the operating batteries

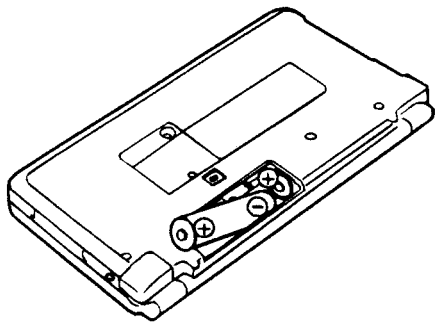
When using the unit, if BATT appears at the top of the display, the operating batteries may need to be replaced. To confirm this, turn the unit off and then on again. If you see "BATT", replace both operating batteries immediately.

To replace the operating batteries;

1. Turn the unit off.
2. Set the battery replacement switch on the back of the unit to "REPLACE BATTERIES" (the red dot will be visible).
3. Slide the operation battery cover off.



4. Remove the old operating batteries.
5. Insert the two new LR6 (AA) operating batteries. Align them correctly for positive (+) and negative (–) polarity, as shown in the battery well.



6. Replace the operation battery cover.
7. Set the battery replacement switch to the "NORMAL OPERATION".

If nothing happens when you press [ON]:

- Setting the battery replacement switch to "REPLACE BATTERIES" shuts off the operating power. Check that the battery replacement switch is set to "NORMAL OPERATION."
- Check that the card lock switch is set to LOCK,
- Repeat the above battery replacement procedure step by step.

3-3. Replacing the memory backup battery

The memory backup battery has an expected lifetime of approximately five years under normal conditions (temperature extremes can shorten this lifetime).
Replace the memory backup battery every five years or whenever the following display appears.

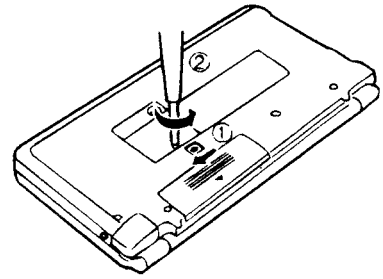
WARNING:
When the operating batteries are depleted, replace them promptly with new batteries. If depleted operating batteries are not replaced, the memory backup battery is drained more quickly than normal.

Memory backup battery lifetime (approx.)

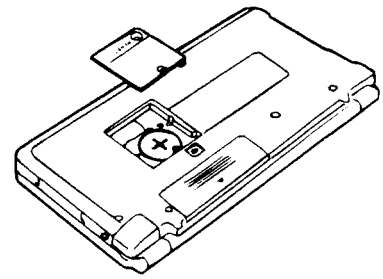
- 2 month (if operating batteries are depleted)
- 5 years (When operating batteries are replaced promptly)

Do not try to replace the memory backup battery if the operating batteries are weak. Doing so may result in the loss of all data in the unit. If necessary, replace the operating batteries before replacing the memory backup battery.

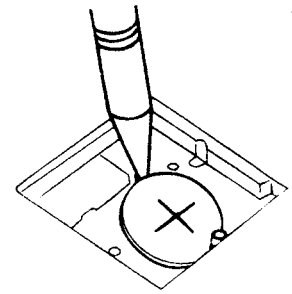
1. Turn off the unit.
2. Set the battery replacement switch on the back to "REPLACE BATTERIES" (a red dot will be visible).
3. Undo the screw from the memory backup battery cover.



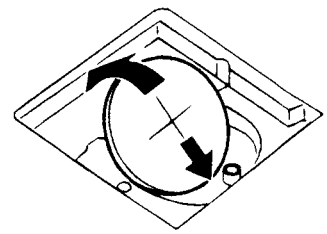
4. Remove the memory backup cover.



5. Remove the old battery using a ballpoint pen or a similar object.



6. Insert a new CR2032 battery, positive (+) side up.



7. Replace the memory backup battery cover and secure with the screw.
8. Set the battery replacement switch to the "NORMAL OPERATION" position.

If nothing happens when you press [ON]:

- Setting the battery replacement switch to "REPLACE BATTERIES" shuts off the operating power. Check that the battery replacement switch is set to "NORMAL OPERATION."
- Check that the card lock switch is set to LOCK,
- Repeat the above battery replacement procedure step by step.

4. Note for repairing

1) When soldering C506 film capacitor (VCFRED2AD473J) manually, the soldering rod temperature and the soldering time must be properly controlled.

- Soldering conditions (Soldering rod)

Soldering temperature	Soldering time	Conditions
260°C Max.	4 sec Max.	• Soldering rod capacity: 30W • Without preliminary heating

(Note)

- Repitition is allowed twice only.
- For remaking after reflow, follow the above conditions.
- Do not use the capacitor which was once removed.

5. Data Exchange

There are many different ways to exchange data, entries, folders, or all entries between your unit and other devices, including Sharp organizers and personal computers. The table below provides a summary of transfer devices, data types, and tasks suited to each device.

(Note)

- Features and capabilities may vary depending upon the Sharp or third party software used.
- Sleep function is disabled in all transfer modes.
- Information about Printer, Fax, RAM card and Flash Memory card, are described in previous sections.
- Use only PC cards (RAM card/Flash Memory card) initialized by a ZR-5000 series. You cannot use PC cards initialized by any other devices, including PCs.

Transfer device	Data and transfer direction (←: from ZR-5000, →: to ZR-5000)			Peripherals required	Recommended tasks
	Main application data	Add-on Software programs	PC Files		
Printer (Refer to Operation manual)	Single entry Entire file/ application Filer folder ←	NA	NA	CE-IR1 + PC Printer Cable None for IrDA compatible printers	Wireless transfer of printer data
Remote fax machine (Refer to Operation manual)	Single Note, Document, Scrapbook entries Filer folders ←	NA	NA	CE-FM4 or PC card modem	Send faxes
RAM Card (Refer to Operation manual)	All entries → ←	NA	Single file All files → ←	NA	Application memory and extra application features
Flash Memory Card (Refer to Operation manual)	All entries → ←	All programs Ä ←	All files → ←	NA	Memory for multiple archive files
Another ZR-5000 series (See 4-1)	Single entry entire file/ applications Filer folders → ←	NA	Single file All files → ←	None for infrared transfer; CE-315L for cable transfer.	Exchange data with other ZR-5000 Series
OZ-5000 OZ-6000 OZ-9000 Series (See 4-1)	Single entry entire file/ applications Filer folders → ←	NA	NA	None for infrared transfer; CE-315L for cable transfer.	Exchange data with Sharp Organizers
Personal computer (Refer to Operation manual)	Single entry entire file/ applications Filer folders → ←	NA	Single file → ←	Software plus:* CE-IR4 or CE-137 + null model cable or Link cable	File transfer with other personal computers
Remote computers, public E-mail services (Refer to Operation manual.)	Differs depending on application			CE-FM4 or PC card modem *	

* Optional software may be required.
NA: Not applicable

5-1. Data Transfer with Other Sharp Devices

Your unit can transfer data with other Sharp Devices as follows:

- ZR5700/5800 to ZR5700/5800 via infrared transfer or cable.
- To/From ZR-5000 via infrared transfer or cable.
- To/From OZ-5000/6000/9000 Series units via infrared transfer or cable.

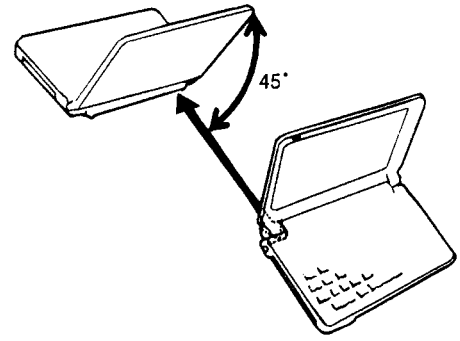
(1) Data transfer between ZR-5700/5800s or with ZR-5000

Data can be transferred easily from one unit to another using the **GET** and **SEND** keys. You can also use SEND Unit to Unit via infrared port or Data Transfer Cable.

- Transfer procedures vary according to whether single entries, folders, files or all entries are transferred.
- Single entries or all entries can be transferred for Activities, Notes, Documents, Outlines, Spreadsheets (between ZR-5700/ZR-5800s only) and Scrapbook.
- Single entries or all file entries can be transferred for Contacts and Data Files.
- Single folders can be transferred from Filer.
- Single file can be transferred for PC Files.
- To transfer whole applications, files, or entries marked as secret, both units must be unlocked.

(2) Wireless infrared transfer (Beaming)

- Wireless transfer is possible with another ZR-5700/ZR-5800, with a ZR-5000 unit or with a OZ-5000/OZ-6000/OZ-9000 series unit.
- No special hardware is required for wireless infrared Unit to Unit transfer.
- The units must be correctly aligned so their infrared ports face each other and are less than 50 cm (20 inches) apart.



- The units should not be more than three-quarters open during transfer or the infrared beam might be blocked.
- No special software setup is required to transfer single entries or folders using the **GET** and **SEND** keys.
- Keep the infrared port clean with a soft, dry cloth.
  Dust on the port restricts data transfer.
- Avoid direct sunlight.
- Infrared transfer is simple, but it is easily affected by ambient conditions such as external light, distance, transfer angle, etc. Received data should be confirmed after the transfer.

(3) Quick transfer

Single entries can be quickly exchanged between two units at any time using the wireless infrared transfer.

To quickly transfer single entries:

1. Turn both units on.
2. On the sending unit, select the entry you want to send in Index mode or View mode.
3. Press **GET** on the receiving unit.
4. Press **SEND** on the sending unit.
   The entry is transferred and added to the proper application data in the receiving unit. It will also be assigned to the IN folder in Filer.

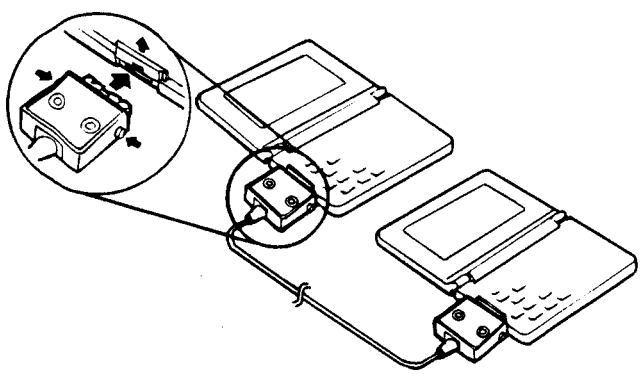
(4) Unit to Unit transfer

① Unit to Unit transfer lets you send:

- Single entries or all entries for Activities, Documents, Notes, Outlines, Spreadsheets and Scrapbook.
- Single entries or all file entries for Contacts and Data Files.
- Single files for PC Files.
- Filer folders.

② For Unit to Unit transfer to take place correctly:

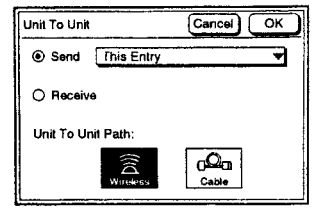
- Both units must use the same path; Cable or Wireless.
- If Cable is selected, connect the optional Data Transfer Cable CE-315L between the two units.



- Check the orientation of the cable when it is connected.
- Disconnect the cable as soon as the transfer is completed to conserve battery power.
- If Wireless is selected, correctly align the two units so that their infrared ports face each other and are less than 50 cm (20 inches) apart.

③ To perform a Unit to Unit data transfer:

1. Open the application.
2. Touch **SEND** and then select **"Unit to Unit"**.



3. Touch **SEND** and select the entry/entries from the pop-up menu.
4. When sending Contacts or Data Files entries, check the With Link Information box as required.
5. Select the Unit to Unit Path from Wireless or cable.
6. When you complete your settings and the other unit is ready to receive data, touch **OK** to transfer the data.

④ To receive a Unit to Unit data transfer:

1. Open the application you want to receive. If you are in the Contacts, Data Files or Holiday, also select the file.
2. Touch **SEND** and then select **"Unit to Unit"**.
3. Select **Receive**.
4. Select Unit to Unit Path from Wireless or Cable.
5. When you complete your settings, touch **OK** and wait for the data to be transferred.
   For detailed steps for the OZ-5000/OZ-6000/OZ-9000 series, see the respective manual.

   Corresponding applications

   When transferring data from your unit to OZ-5000/6000/9000 series, the following applications correspond:

   Schedule - Appointment
   To Do - To Do
   ANN 1 - Holiday (Yearly by date)
   ANN 2 - Holiday (Yearly by day)
   Tel 1 - Contact 1
   Tel 2 - Contact 2
   Tel 3 - Contact 3
   User File 1 - Data File 1
   User File 2 - Data File 2
   User File 3 - Data File 3
   Notebook, Memo - Documents
   Outline - Outlines
   Scrapbook - Scrapbook

   - For Appointments, Contacts and Data Files entries, if the Filter function is turned on, only filtered entries are sent. For Filer, transferred entries are stored in the proper source applications and are also automatically assigned to the IN folder on the receiving unit. After the transfer, move IN folder data to another folder.
   - When transferring data from the OZ-5000/OZ-6000/OZ-9000 series to the ZR-5700/ZR-5800 from an application in different format, a warning message may be displayed.
     You should check whether all the data was transferred successfully after selecting **OK**.

⑤ Transfer conditions

- Press **ON** at any time to cancel a transfer.
- Received data is stored and appended to existing data in the selected application.
- After a transfer using **GET** and **SEND** on the keyboard, the data is also automatically assigned to **Filer**'s IN folder so that you can check it.
  Always try to keep the IN folder empty.
- If a RAM card is installed and selected as the data source, data in the card can also be selected for data transfer.
- For **Contacts** or **Data Files**, the receiving file must be set up with the same fields. If a filed type (text or picture) is different, the field cannot be transferred.
- Be sure that the sending unit does not have a blank (no characters) Telephone/Contact or User File/Data File *field name* or else the ZR-5700/ZR-5800 will not be able to receive information (an error message will appear).
- **GET** and **SEND** on the keyboard do not work for cable transfers. These keys initiate an infrared transfer regardless of the selection for Unit to Unit path or if a cable is connected.

5. FLASH-EEPROM SERVICE WRITING/CHECKING PROCEDURES

The procedures are for writing into the FLASH-EEPROM in the ZR-5700/5800.
Servicing for the ZR-5700/5800 is performed in the following cases:

① When the Main PWB unit is replaced.

② When Main ROM PWB is replaced.

③ When the FLASH-EEPROM version is updated.

Introduction

The PCMCIA card making procedures are described hereinafter which are used to write into the 4Mbit FLASH-EEPROM provided in the ZR-5700/5800 (ROM version 1.0 or later).
The procedures are classified into the following three groups:

(1) Install the PCMCIA card making software into the ZR-5700/5800 (*1).

(2) Make one PCMCIA card with the installed software.
The card includes the software to revise the contents of the 4MBit FLASH-EEPROM provided in the ZR-5700/5800 (ROM version 1.0 or later).

(3) Use the PCMCIA card made in procedure (2) to revise the contents of the 4Mbit FLASH-EEPROM provided in the ZR-5700/5800 (ROM version 1.0 or later).

5-1. Installation of the card making software

1) Outline

This software for making PCMCIA cards which are used to revise the contents of the 4Mbit FLASH-EEPROM provided in the ZR-5700/5800 (ROM version 1.0 or later) is installed.

2) Necessary devices

- ZR-5700/5800 (*1), 1 unit
- AC adapter (EA-23E) for ZR-5700/5800, 1 unit
  IBM-PC (compatible machine): With the MS-DOS (*2) installed in the hard disk.
- RS-232C level convertor (CE-131T or CE-137T): To use the CE-131T, the AC adapter (EA-11E) is required.
- RS-232C cable
- Floppy disk: 1 pc. (*3): Check the label.

ZR-5700/5800 ROM V1.0 or later FLASH-EEPROM writing card making software Ver0.0 mm/dd/yy

Disk content:

"INSTALL.BAT": Batch file for installation executed in MS-DOS.
"Z58P_Vxx (*4).EXE": File used by "INSTALL.BAT."

(*1): This is not the user's set. It is used to make a card. Any ROM version will do.

(*2): Trademark of Microsoft.

(*3): Supplied by SHARP. In the future, it may be supplied through the communication network instead of by a floppy disk.

(*4): "xx" shows the version number.

3) Operating procedure

1. Connect the devices as shown below:
   Fig. 1-1 shows the case where the level converter CE-131T is used.
   Fig. 1-2 shows the case where the level convertor CE-137T is used.

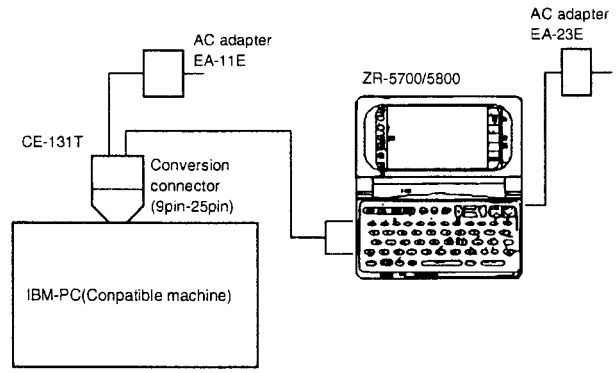


Fig. 1-1: Connection diagram (when the CE-131T is used)

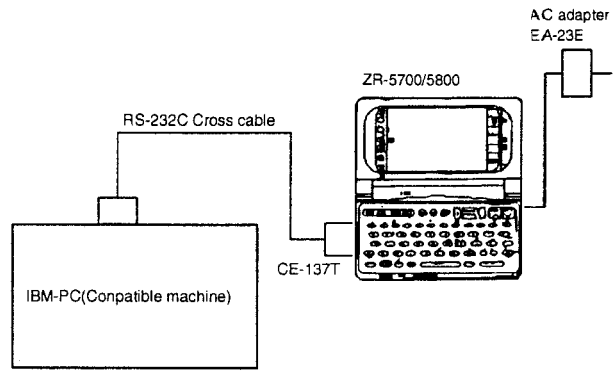


Fig. 1-2: Connection diagram (when the CE-137T) is used)

2. Turn on the power of the IBM-PC (compatible machine) to start the MS-DOS. (The MS-DOS command prompt appears.)
3. Make a working directory on the MS-DOS.
4. Copy "INSTALL.BAT" and "Z58P_Vxx.EXE" in the floppy disk into the directory made in the above procedure.
5. With the ON key on the ZR-5700/5800 keyboard pressed, push the reset button on the back side.
6. Touch "Yes" on the screen of the ZR-5700/5800 LCD as shown below.

Do you really want to initialize the main memory (this will delete all main data)? Yes No

7. Type "INSTALL.BAT" and press the ENTER key of the IBM-PC (compatible machine).
The batch file is executed and the PC screen shows the following display (Fig. 3).

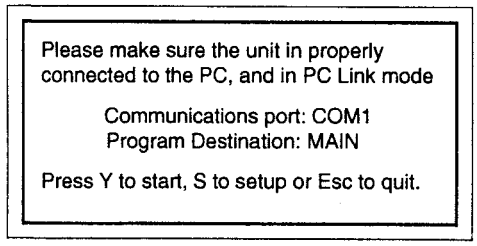

Please make sure the unit in properly connected to the PC, and in PC Link mode
Communications port: COM1
Program Destination: MAIN
Press Y to start, S to setup or Esc to quit.

Fig. 3

8. Check that the display shows as follows:

```
Communications port: COM1
Program Destination: MAIN
```

If not, press "S" key of the IBM-PC keyboard, and follow the instructions for setting.

9. Touch "TOOLS" on the ZR-5700/5800 touch panel. The display shows as shown in Fig. 4.

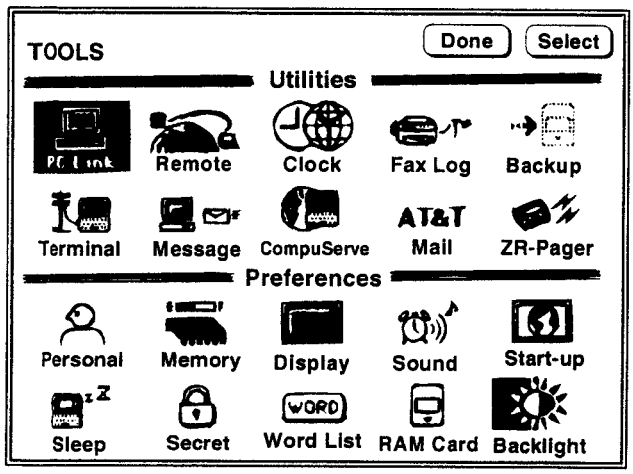


Fig. 4

10. Touch "PC Link" icon. The display shows as shown in Fig. 5.

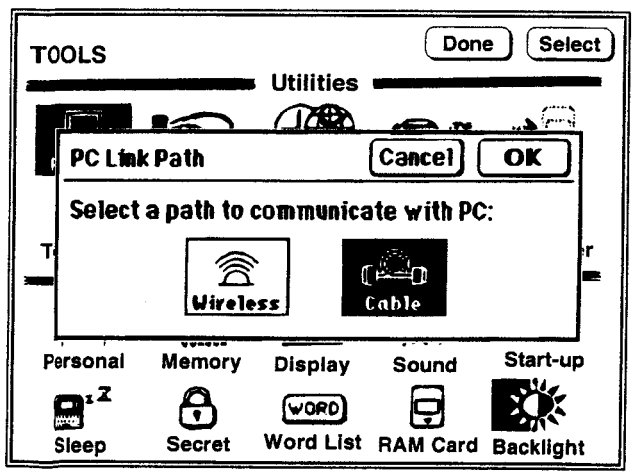


Fig. 5

11. Touch "Cable" in Fig. 5 and touch "OK." Check that the display shows as shown in Fig. 6.

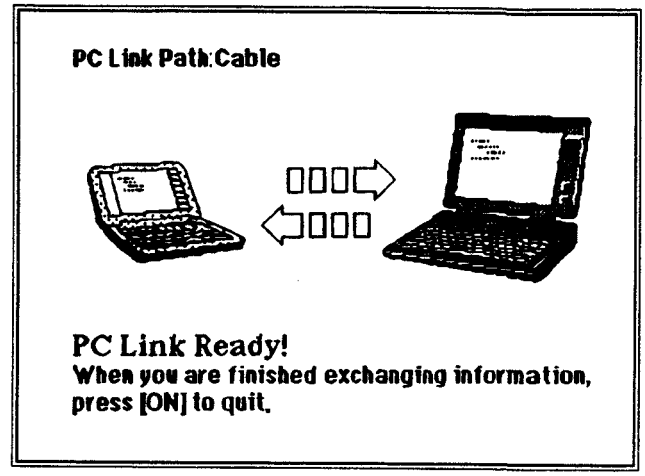


Fig. 6

12. Press "Y" key of the IBM-PC keyboard. The monitor shows as shown in Fig. 7.

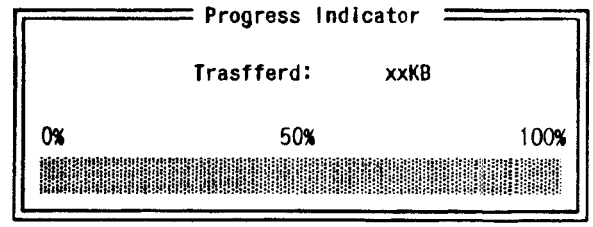
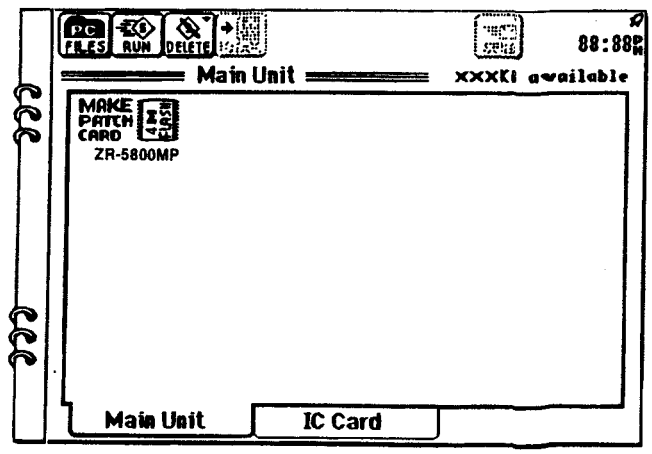


Fig. 7

13. After completion of transmission, the IBM-PC returns to the MS-DOS prompt.
The ZR-5700/5800 is resumed automatically.

14. After the ZR-5700/5800 is resumed, touch "More" on the touch panel. Check that the "MAKE PATCH CARD" icon is displayed. (Fig. 8)



Note: The icon design may be modified.

Fig. 8

5-2. Making of the ZR-5700/5800 4Mbit FLASH-EEPROM writing card

1) Outline

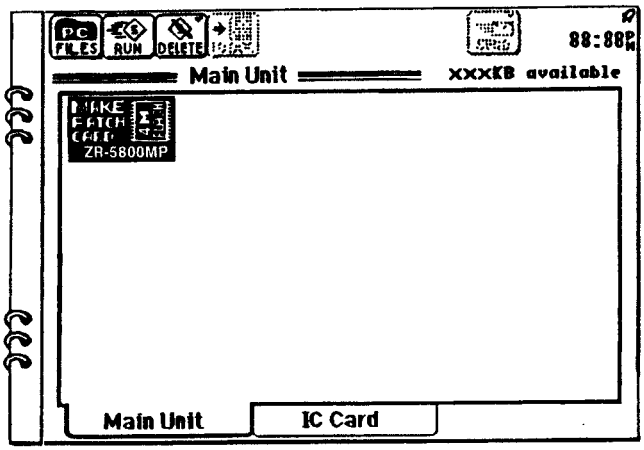
The software installed in procedure 5-1 is used to make a PCMCIA card. This cars has a function to revise the content of the 1Mbit FLASH-EEPROM provided in the ZR-5700/5800 (ROM version 1.0 or later).

2) Necessary devices

- ZR-5700/5800 (*1): 1 unit to which the software is installed in "1) installation of the card making software."
- AC adapter (EA-23E) for ZR-5700/5800: 1 unit
- PCMCIA FLASH card (Sharp CE-AF1 is recommendable.)

3) Operating procedures

1. Connect the AC adapter.
2. Press the ON key of the ZR-5000 to turn on the power.
3. Touch "MAKE PATCH CARD" icon twice. (Refer to Fig. 9.)



Note: The icon design may be modified.

Fig. 9

5. Check that the display shows as shown in Fig. 10, and insert the FLASH card properly.

```
"ZR-5700/5800 4Mbit FLASH writing card" maker
Version x.x
Please insert PCMCIA FLASH card.
```

Fig. 10

6. Wait until "now working... Please wait." disappears. (Refer to Fig. 11.)

```
"ZR-5700/5800 4Mbit FLASH writing card" maker
Version x.x
Now working... Please wait.
```

Fig. 11

7. Check that the display shows as shown in Fig. 12. Set the write protect switch of the PCMCIA card to the protect side, and eject out the PCMCIA card.

```
"ZR-5700/5800 4Mbit FLASH writing card" maker
Version x.x
Writing was finished successfully.
Please eject the card.
```

Fig. 12

After ejecting the PCMCIA card, the display shows as shown in Fig. 10.

8. To make another card, repeat procedures 5 - 7.

   * To terminate the operation, push the reset button on the back side.

5-3. Rewrite procedure of 4MBit FLASH-EEPROM in the ZR-5700/5800 (ROM version 1.0 or later)

1) Outline

The PCMCIA card made in the above procedure 5-2) is used to rewrite the content of the 1MBit FLASH-EEPROM provided in the ZR-5700/5800 (ROM version 1.0 or later).

2) Necessary devices

- ZR-5700/5800 (*1): 1 unit to revise the FLASH content.
- AC adapter (EA-23E) for the ZR-5700/5800: 1 unit
- PCMCIA FLASH card made in "ZR-5700/5800 4MBit FLASH-EEPROM writing card 2)."

3) Operating procedures

Before the operation, be sure to backup the user data.
After completion of the operation, restore the user data, adjust the clock, and return the unit to the user.

1. Connect the AC adapter.
2. Insert the PCMCIA FLASH card "ZR-5700/5800 4MBit FLASH-EEPROM writing card" into the PCMCIA slot.
3. With the ON key and the D key pressed, push the reset button on the back side.
4. Check that the diag.menu is displayed. With the ON key and the V key pressed, push the reset button on the back side.
5. Check that the display shows as shown in Fig. 13.

```
** ZR-5700/5800 4Mbit FLASH installer **
ROM version x.x
Patch version x.x
Now working... Please wait.
```

Fig. 13

6. Check that the display shows as shown in Fig. 14, and press the OFF key of the ZR-5700/5800.

```
** ZR-5700/5800 4Mbit FLASH installer **
ROM version x.x
Patch version x.x
Installation OK.  Please [OFF] key

check sum = xxxx
```

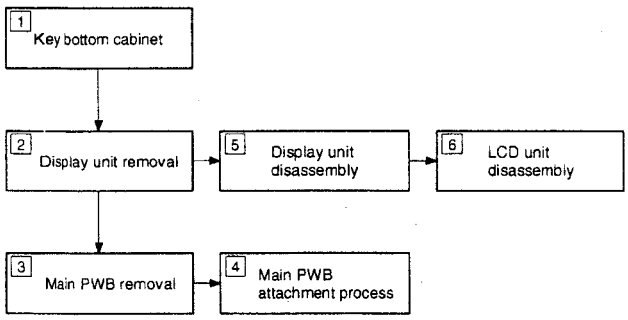
Fig. 14

7. Disconnect the AC adapter.
8. Eject the PCMCIA card.

CHAPTER 4. DISASSEMBLY AND ASSEMBLY

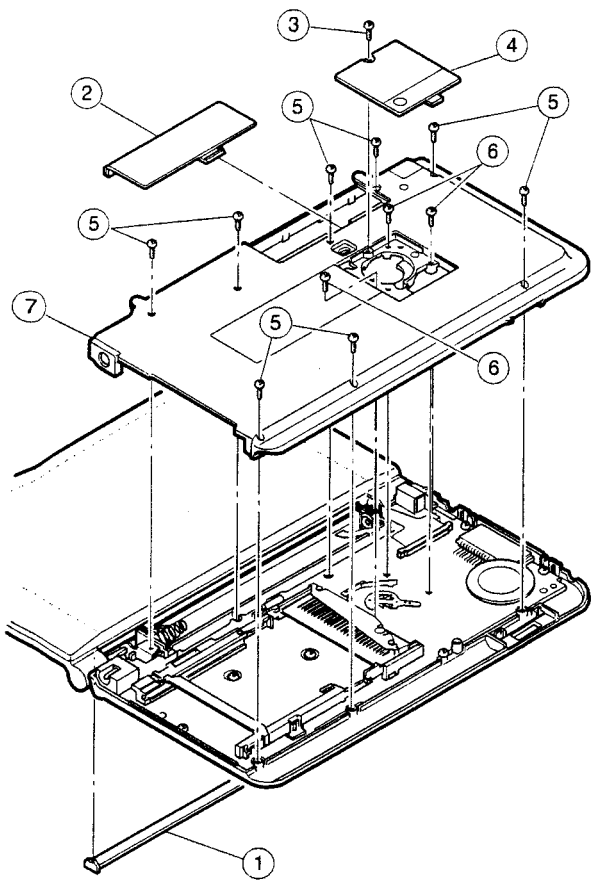
This chapter mainly describes the disassembly procedure. For assembly, reverse the disassembly procedures. If any special care is required for assembly, "Note for assembly" is provided.
Simple and easy replacement procedures of units and parts are omitted.

[Flowchart of disassembly]


1 Key bottom cabinet
2 Display unit removal
5 Display unit disassembly
6 LCD unit disassembly
3 Main PWB removal
4 Main PWB attachment process

1 Key bottom cabinet removal

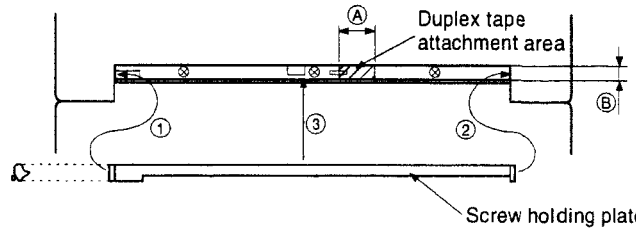
1. Remove screw holding plate ①.
2. Remove battery cover ②.
3. Remove screw ③ and remove battery cover ④.
4. Remove eight screws ⑤ and three screws ⑥, and remove key bottom cabinet ⑦.



[Note for assembly]

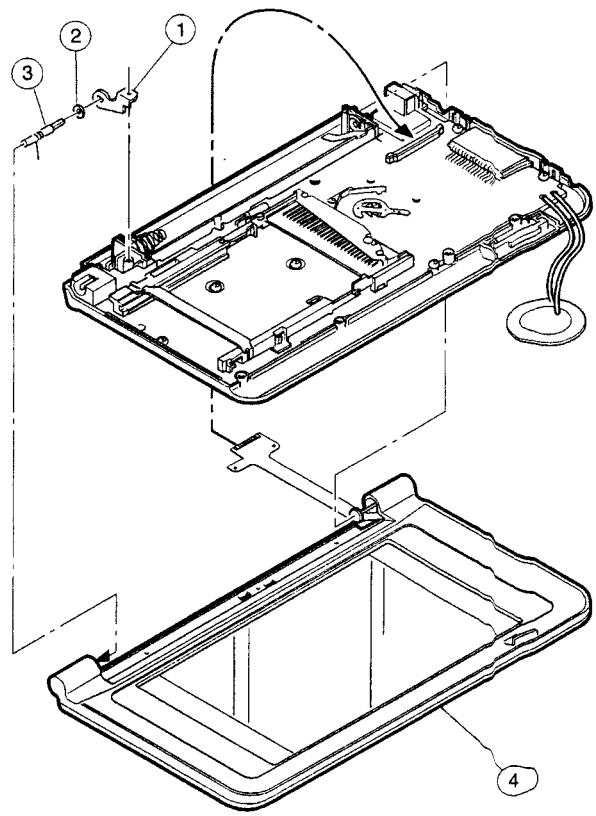
1. Screw holding plate/duplex tape attachment

1) Duplex tape must be attached within the range of Ⓐ and Ⓑ as shown in the figure below. (Do not allow the tape to extend from the shaded area.)
2) Fix the screw holding plate in the sequence of ① → ② → ③ so that it is levelled.



2 Display unit removal

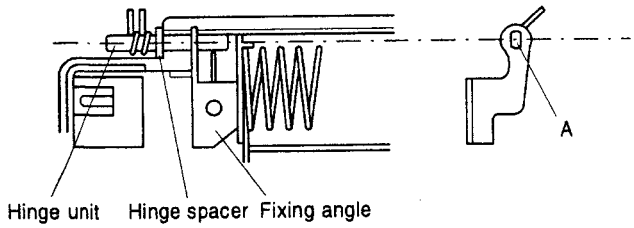
1. Remove hinge fixing angle ①.
2. Remove hinge spacer ② and remove hinge unit ③.
3. Remove display unit ④.



[Note for assembly]

1. Hinge fixing angle/hinge unit/hinge spacer attachment

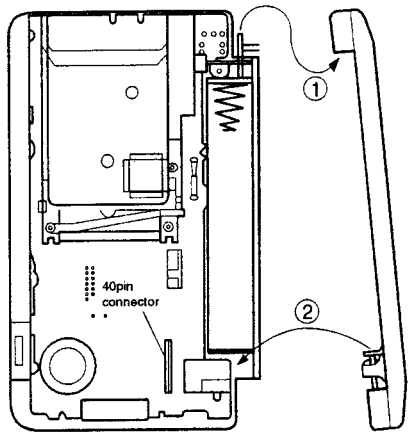
When inserting the hinge unit into the fixing angle, fit the shapes at position A in the figure below.

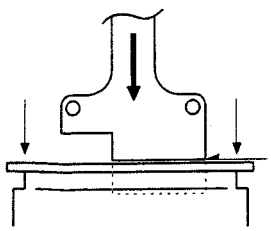


2. Connection of the display side and the key side

1) Hold the key side and the display side apart 90° each other with both hands. Press the fixing angle of the key side with fingers and insert ① and attach ②. (Fit the angle at the spring tip of the hinge unit and the hole in the hinge section of the key side.)
2) After connecting them, close the key side and the display side slowly.
3) Press the fixing angle onto the PWB.
4) Check that the FPC section is not squeezed (free from wrinkles). Temporarily fix it, release lock of 26-pin connector of the main PWB, insert the FPC, and lock it with a lock jig.

(Note) When assembling ②, be careful not to make contact between the FPC and the cabinet pawl.

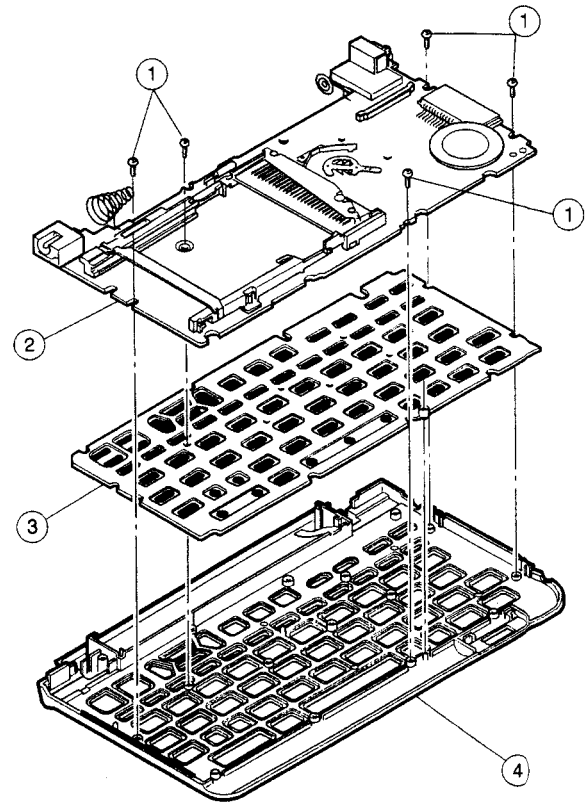




With the 26pin connector released, insert the FPC until the white backup tape is almost covered, and lock it.

3 Main PWB removal

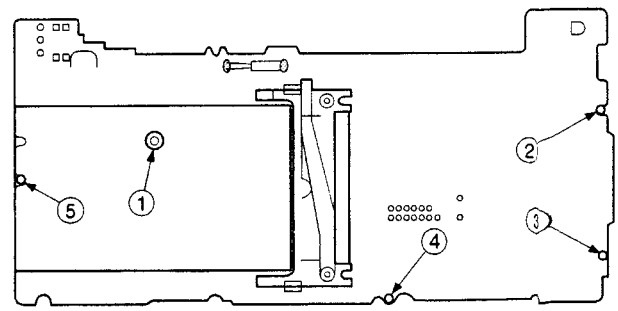
1. Remove six screws ①.
2. Remove main PWB ②.
3. Remove key rubber ③ from key top cabinet ④.



[Note for assembly]

1. Main PWB screw tightening

Tighten the screws in the sequence shown below.



Tightening torque: 0.7 ± 0.1 kg.cm

2. From attachment of the sounding body to engagement of the cabinet

1. Remove the separation sheet (shaded portion) of the sounding body fixing tape from the slit.
2. Place the sounding body to that it fits with the removed separation sheet shape, and attach it.

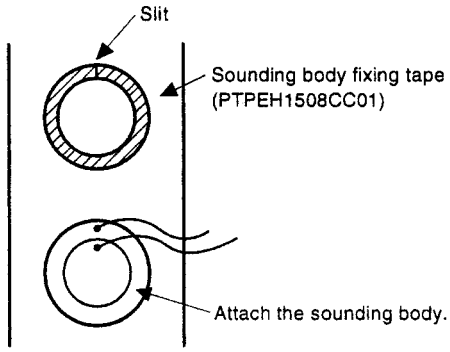


Fig. 1

3. Attach the sounding body with the tape attache to it to the attaching reference as shown in Fig. 2.
   At that time, arrange so that the lead solder section of the sounding body comes to the position shown in the figure.

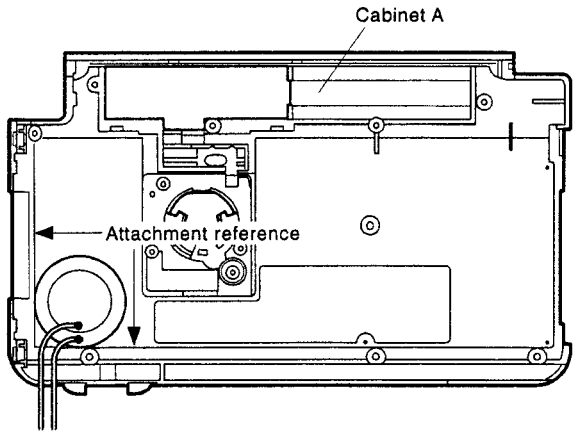


Fig. 2

4. Arrange the cabinet as shown in Fig. 3, and solder the red lead wire to R pad, and the black lead wire to B pad. (R and B are marked on the PWB soldering pads.)

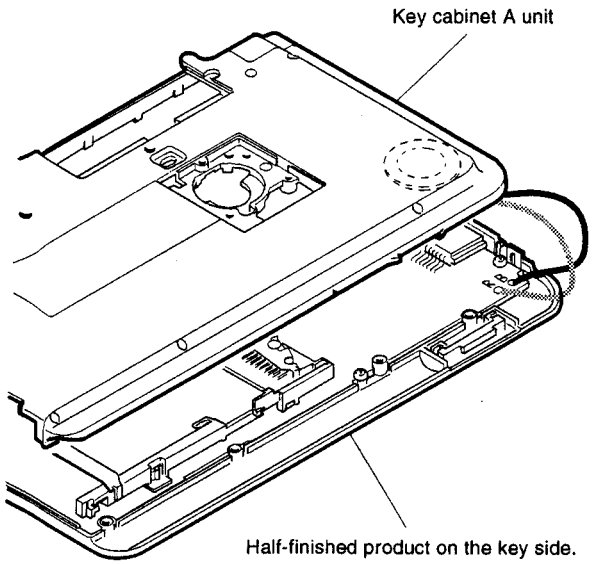
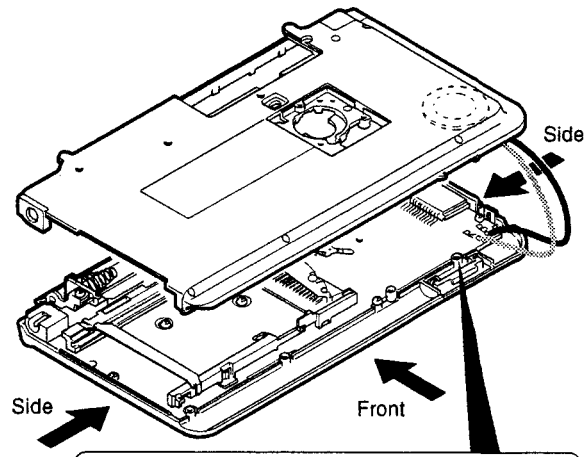


Fig. 3

5. To engage the cabinet A unit, first engage the battery box side as shown in Fig. 4, and push the lead wire inside with your fingers. Then engage the both sides and the front side. Guide the lead wires as shown in Fig. 5.



* Arrange the lead wire as shown in the figure so that it may not be squeezed by the screw fixing boss.

Fig. 4

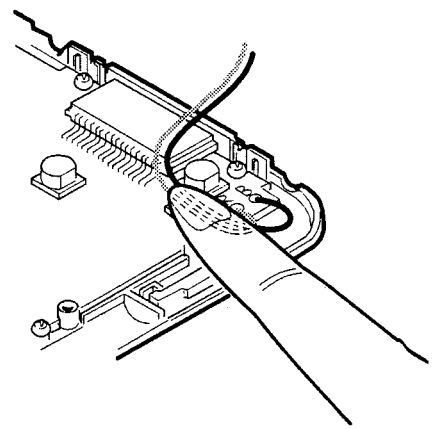
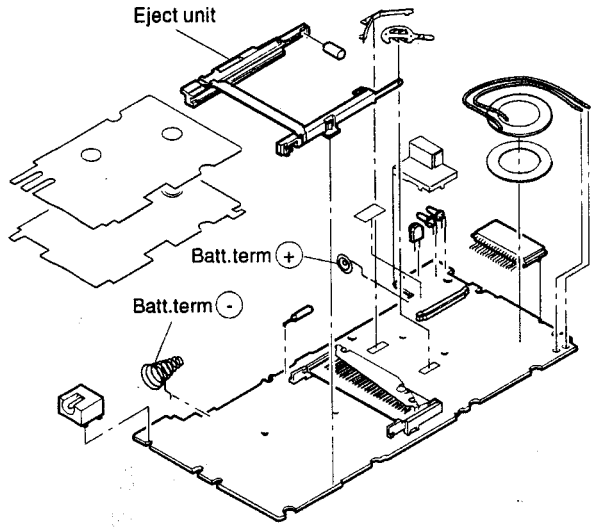


Fig. 5

4 Main PWB attachment process



[Note for assembly]

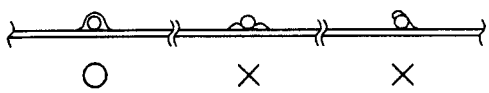
1. General precautions

- When handling the PWB, perform the preventive measures against static electricity. (Grounding band, humidifier, etc.)
- Do not touch the contact pattern of the PWB with bare hands. (Use finger sucks or gloves.)
- Be sure to insert the soldered sections firmly into the PWB. (Must be free from floating, slant, shift, etc.)
- When handling the PWB, do not apply a mechanical or electrical stress.
  The soldering conditions are as follows unless otherwise specified:
  Solder tip temperature(effective): Max. 300°C
  Soldering time: Max. 3 sec

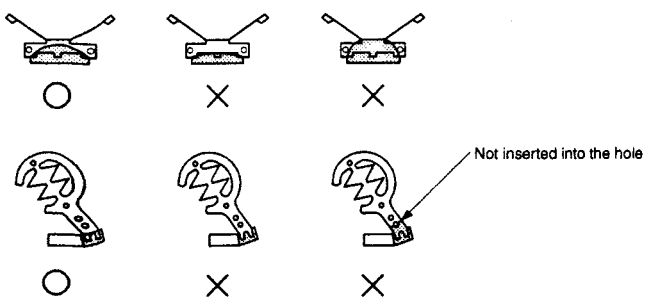
2. Main battery terminals (+)(–) soldering (with a jig)

Soldering conditions:
Solder tip temperature: Max 350°C
Soldering time: 3 ~ 5 sec (Be sure to solder securely.)

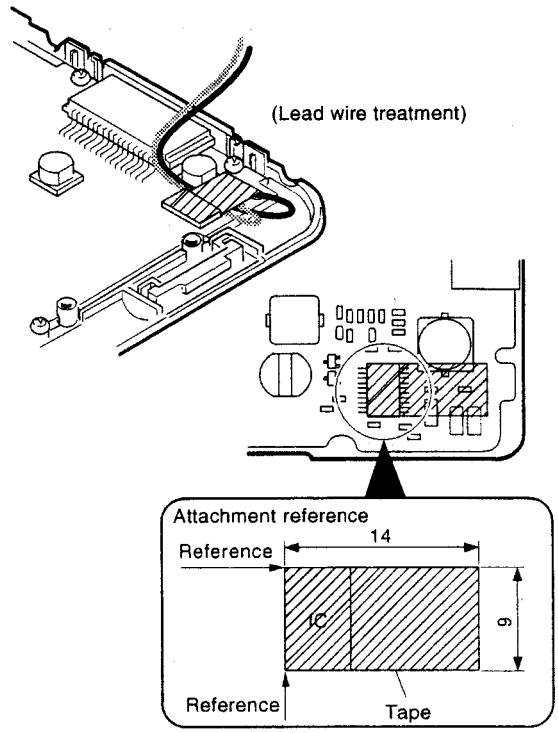
[Soldering portion cross sectional view]



3. Backup battery (+)(–) soldering (with a jig)



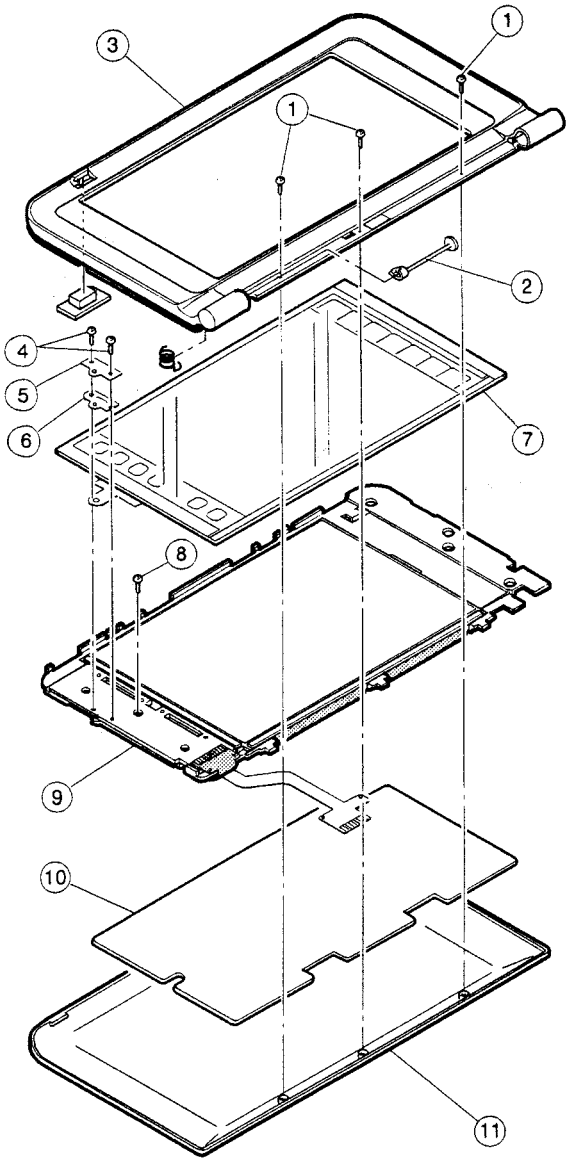
4. Sounder attachment/soldering/wire treatment



- When attaching, fit with the mark shown with the arrow in the figure.
- Attach to the shaded portion in the figure above. (Do not press the other sections.)
- Keep the sounder lead wire away from the 15-pin connector.

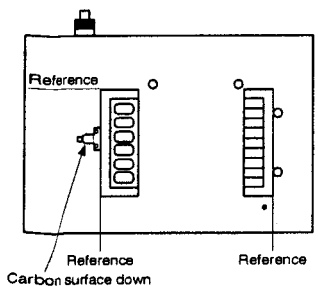
5 Display unit disassembly

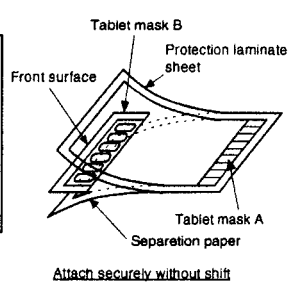
1. Remove three screws ①.
2. Remove hinge pin ②, and remove display upper cabinet ③.
3. Remove two screws ④, pressure angle ⑤, and pressure rubber ⑥.
4. Remove tablet unit ⑦.
5. Remove LCD unit ⑧.
6. Remove supporting plate ⑨ and display bottom cabinet ⑩.



[Note for assembly]

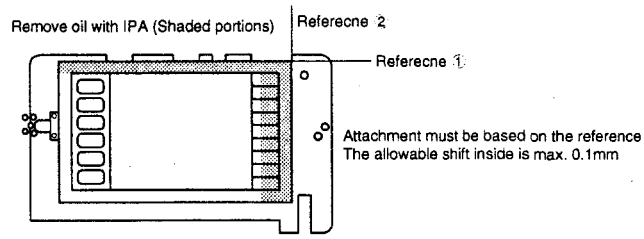
1. Tablet/tablet mask attachment





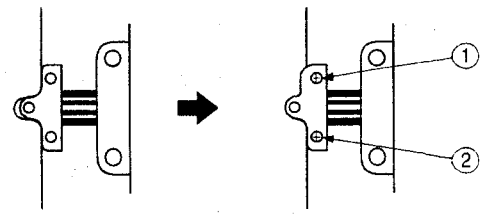
2. Tablet unit attachment

(Note) Clean and remove oil from the LCD holder tablet attachment surface.


Remove oil with IPA (Shaded portions)
Referecne 2
Referecne 1
Attachment must be based on the reference
The allowable shift inside is max. 0.1mm

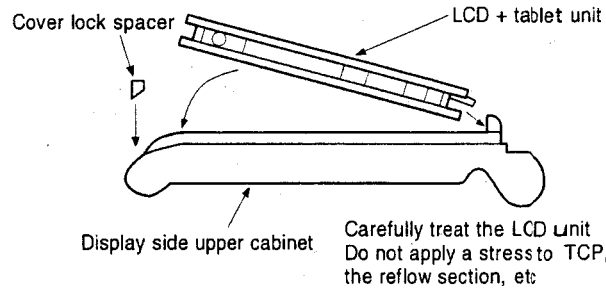
Fit the tablet unit with reference 1, attach it along reference 2
Be sure to perform air blow and check the external view

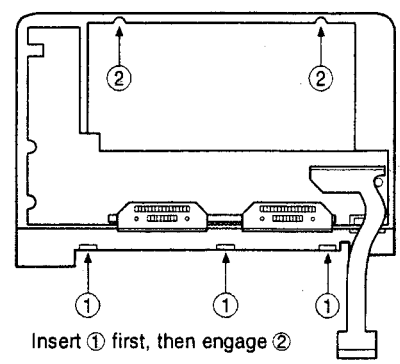
3. Pressure rubber/pressure angle attachment and fixing



Screw tightening torque: 1.3±0.1Kgcm
Tighten the screws in the sequence of ① then ②

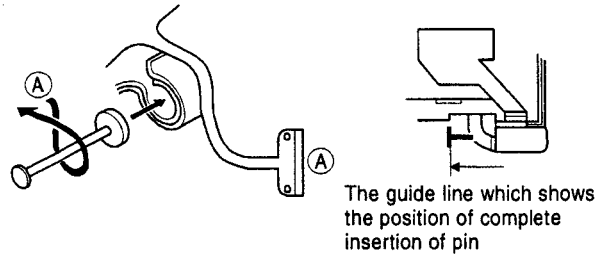
4. Cover lock spacer/LCD tablet unit attachment


Cover lock spacer
LCD + tablet unit
Display side upper cabinet
Carefully treat the LCD unit
Do not apply a stress to TCP, H/S, the reflow section, etc



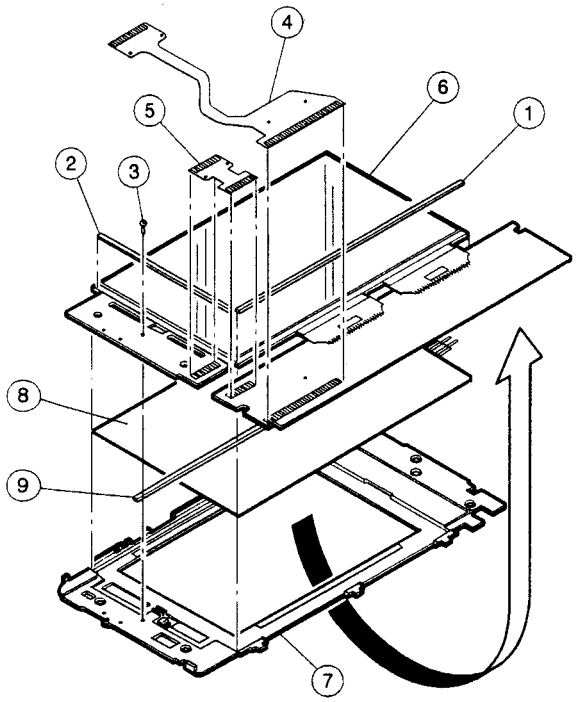
Insert ① first, then engage ②

5. Hinge pin attachment/FPC process



6 LCD unit disassembly

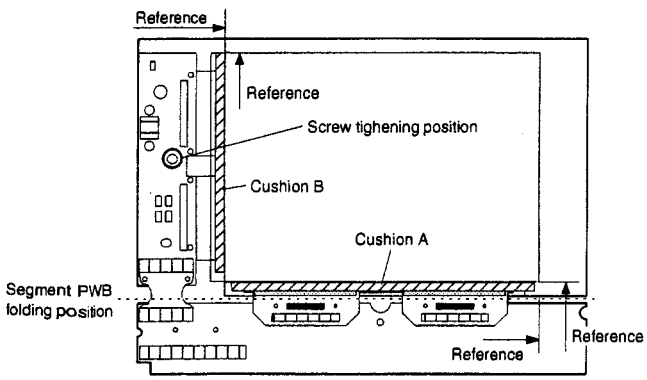
1. Remove LCD cushion A ① and LCD cushion B ②.
2. Remove screw ③.
3. Disconnect FPC B ④ and FPC A ⑤.
4. Remove H/S unit ⑥ from LCD holder ⑦.
5. Remove EL panel ⑧ and LCD fixing tape ⑨. (ZR-5800 only)



[Note for assembly]

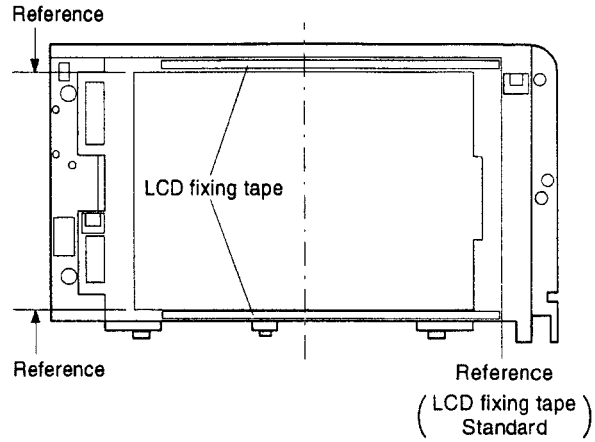
1. Cushions A & B attachment/screw tightening/segment PWB folding

1) Do not extend cushions A & B from the reference lines. Do not allow them to cover the LCD side.
2) Fold the segment PWB inside.



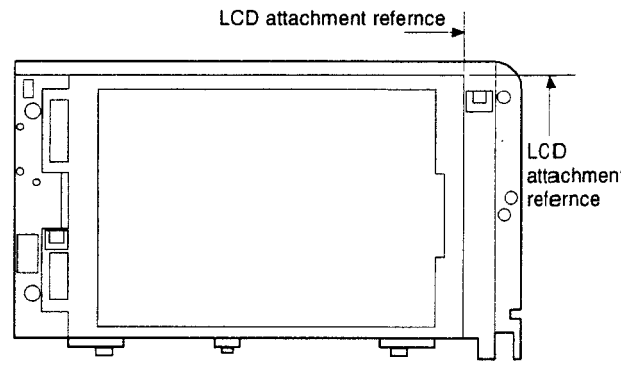
2. LCD fixing tape attachment

1) Attach the LCD fixing tape by fitting it with the LCD holder center and the reference as shown below:
2) Do not extend from the reference and do not cover the LCD holder vertical surface.

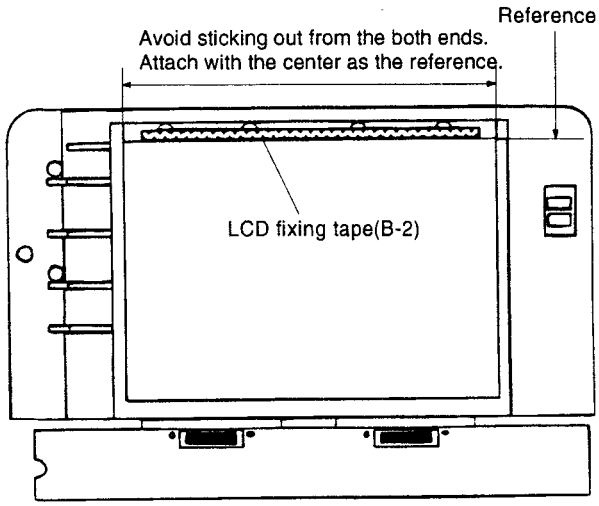


3. LCD attachment

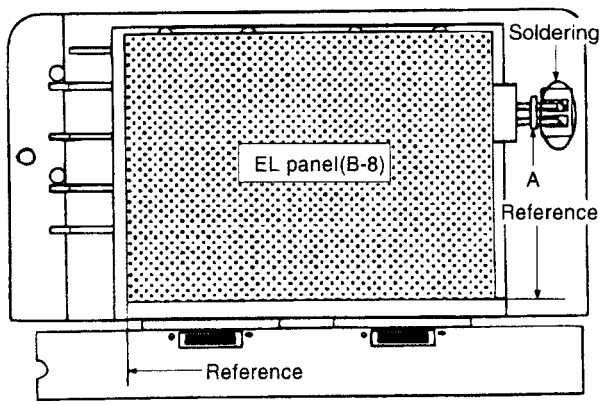
1) Attach the LCD to the right upper reference of the LCD holder as shown below:
2) Allowable shift is 0 ~ 0.1mm.
3) Do not cover the LCD.



4) Attach the LCD fixing tape and the EL panel fixing tape. (ZR-5800 only)



[LCD fixing tape attachment] (ZR-5800 only) (Fig.1)



[EL panel soldering] (ZR-5800 only) (Fig.2)

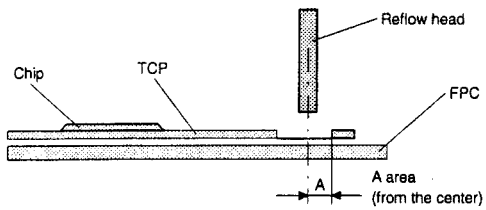
7 Reflow

1. Note for reflow

1) Reflow

① The reflow conditions specified in the following are used as the reference only. In actual, visually check the soldering state.

② Check the reflow position.

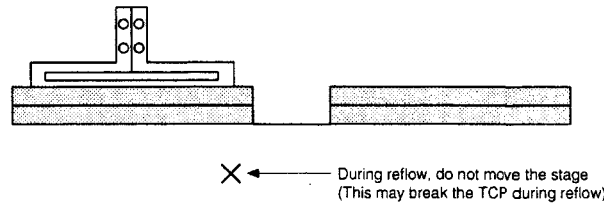


* Check that the reflow head is not over the base film (TCP)
* Adjust so that the reflow head is not shifted to the chip side (This may cause breakage of the lead wire)

2) Precautions

① Always check that the reflow head is not over the base film.

② Check that the reflow head position is not shifted extremely to the chip side. (This may cause breakage of the TCP lead wire.)



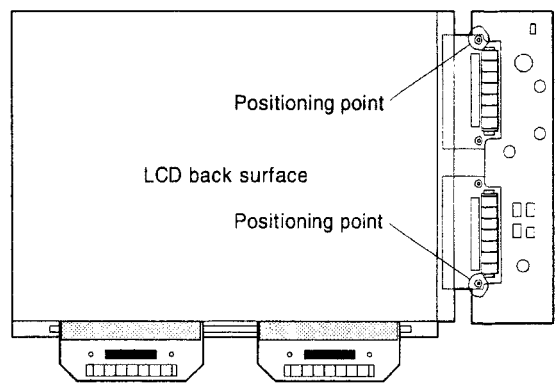
2. Common TCP reflow outline

1) Apply flux to the common reflow terminal of the common PWB.

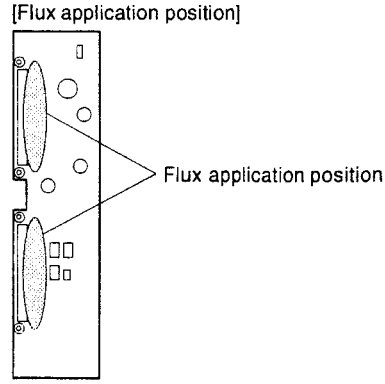
2) Position the TCP as shown below (2 positions):

(Pre-scale judgement)

[Reflow position]



[Flux application position]



3) Reflow conditions: Temperature/time setting

1st	200°C ~ 2sec
2nd	340°C ~ 8sec

[Note]

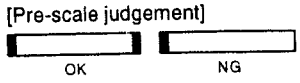
① Apply flux to the whole terminal.

② Do not apply an stress to the TCP chip, the flex, and the reflow section.

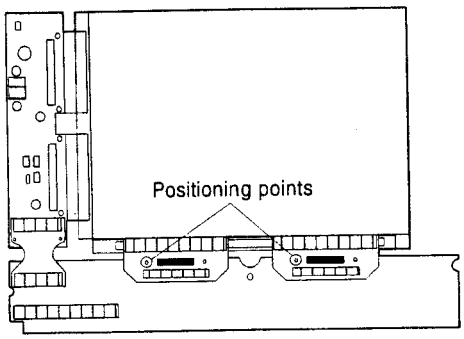
3. Segment TCP reflow outline

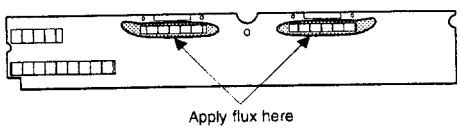
1) Apply flux to the segment reflow terminal of the segment PWB.
2) Position the TCP as shown below (2 positions):

[Pre-scale judgement]



[Reflow position view]





[Flux appling position]

3) Reflow conditions: Temperature/time setting

1st	200°C ~ 2sec
2nd	300°C ~ 8sec

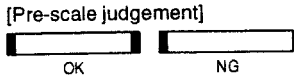
[Note]

① Apply flux to the whole terminal.
② Do not apply an stress to the TCP ship, the flex slit, and the reflow section.

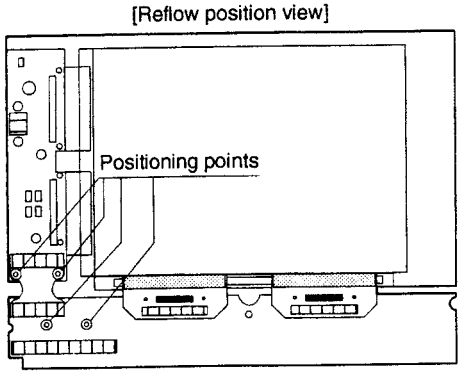
4. Connection FPC A reflow outline

1) Apply flux to the reflow terminal of the common segment PWB.
2) Position h connection FPC A as shown below:

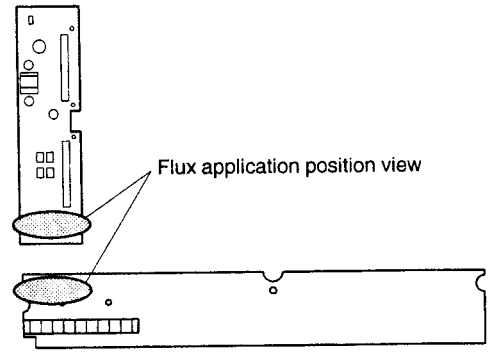
[Pre-scale judgement]



[Reflow position view]



[Flux application position view]



3) Reflow conditions: temperature/time setting

1st	180°C ~ 2sec
2nd	390°C ~ 8sec

[Note]

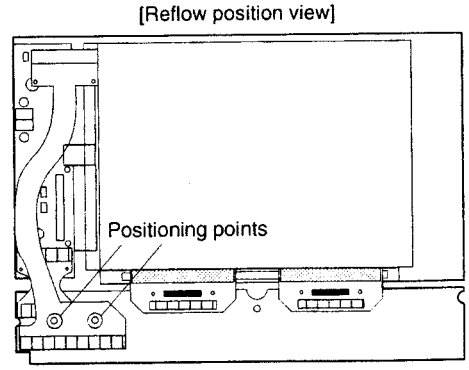
① Apply flux to the whole terminal.

5. Connection FPC B reflow outline

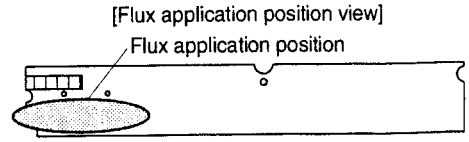
1) Apply flux to the reflow terminal of the segment PWB.
2) Position the connection FPC as shown below (2 positions):

[Pre-scale judgement]

[Reflow position view]



[Flux application position view]



3) Reflow conditions: temperature/time setting

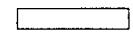
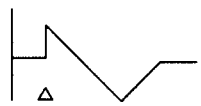
1st	180°C ~ 2sec
2nd	350°C ~ 8sec

[Note]

① Apply flux to the whole terminal.

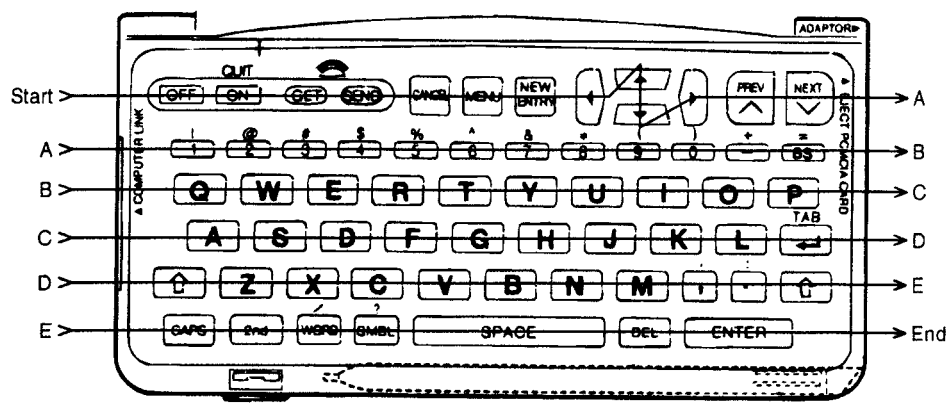
CHAPTER 5. DIAGNOSTICS AND CHECK ITEMS

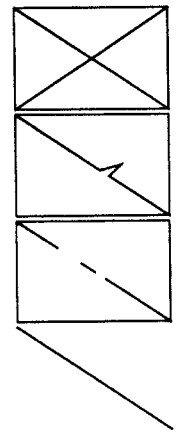
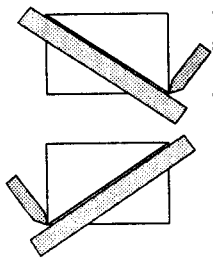
* Note: When the diagnostics is started, the other test menu program is also started. In servicing, use only "7. CHECK PRODUCT (AFTER)" and do not touch the other programs. (It touched, the system program of the main unit may be deleted.)

No.	Operating procedure	Display	Check item
1	Enter the diag mode with ON + D + RES.	Diag menu *	
2	Touch "7. CHECK PRODUCT (after)."	Frame display 	Check for no defects.
3	Press the ENTER key.	Plover A	Check the display for no defects and blurs. Perform the shock test and the twist test with plover A.
4	Press the ENTER key.	Plover B	Check the display.
5	Press the ENTER key.	Plover C	Check the display.
6	Press the ENTER key.	Plover D	Check the display.
7	Press the ENTER key.	Rain fall	Check the display for no blurs under the lines.
8	Press the ENTER key.	Plover A with fluctuated density 	Check that the display density changes smoothly.
9	Automatic operation	*** LCD CHECK *** LCD register CHECK << CHECK OK >>	Check the display of "CHECK OK."
10	Automatic operation	Vertical stripe → VRAM CHECK	Check the display of ""LCD CHECK OK" and "VRAM CHECK OK."
11	Automatic operation	*** CHECK ROM *** << CHECK OK >> ↓ *** CHECKING RAM *** ↓ *M byte RAM << CHECK OK >> ↓ *** ALARM CHECK *** RTC REGISTER OK << ALARM CHECK !! >> ↓ RTC REGISTER OK ALARM 1 OK << ALARM CHECK !! >> ↓ RTC REGISTER OK ALARM 1 OK ALARM 2 OK << CHECK OK >>	Check that all tests result in "CHECK OK." * ZR5700 → 1MB ZR5800 → 2MB
12	Automatic operation	*** KEY CHECK *** << CHECK OK >>	Check the display of "CHECK OK." (See below figure.)

KEY LAYOUT

KEY CHECK



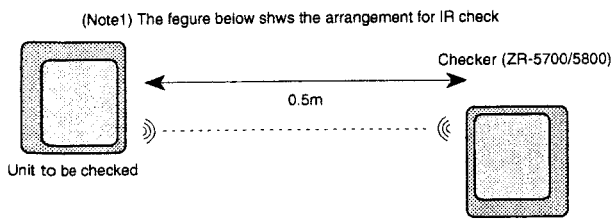
No.	Operating procedure	Display	Check item	
13	Press the ENTER key. Touch [+] at the left upper side. Touch [+] at the right lower side.	Left upper [+] Right lower [+] (Refer to [Note](1).)		Draw a straight line without deflection. If the line deflects, put a slightly stronger pressure on the pen and draw a line again. If the line is cut out, move the pen more slowly and draw a line again. If there is a shift between the line and the pen, perform the tablet check from the beginning to check again.
14	Draw two lines; left upper right lower, and left lower right upper.  Put a scale on the screen (left upper right lower) and draw a line. Draw a line from left lower to right upper side similarly.	(Note) Use a hard, plastic ruler, and use the attached pen. Draw a line slowly and similarly with normal writing with a pencil.		
15	Press the ON key.	** CHECK OPT-COM(ASK) ** <<< CHECK OK >>>	Check the display of "CHECK OK."	Checker unit (ASK & IRDA, MASTER) must be in the standby mode. (Refer to [Note] (2).)
16	Press the ON key.	** CHECK OPT-COM(IRDA) ** <<< CHECK OK >>>	Check the display of "CHECK OK."	
17	Press the ON key.	** CHECK 15PIN ** <<< CHECK OK >>>	Check the display of "CHECK OK."	Since the 15pin check in diagnostics requires a checker, use the PCMCIA check procedure of [NOTE] (3).
18	Press the ON key.	** CHECK PCMCIA ** check PCMCIA controller <<< CHECK OK >>>	Check the display of "CHECK OK."	
19	Press the ON key.	** CHECK PCMCIA ** <<< CHECK OK >>>	Check the display of "CHECK OK."	

Shock test: With the unit open, drop it from a height of 10 cm in parallel twice, and check that there is no abnormality in the operation and the display.
Twist test: Twist the unit (key side) and check that there is no abnormality in the operation and the display.

[Note]

(1) When performing No. 13 tablet adjustment, press the center of [+] correctly. The adjustment value at that time is written into the flash memory when setting the proper density.

(2) The figure below shows the arrangement for IR check.



(3) PCMCIA connector check procedure

Necessary tool: CE-AR1 (1MB SRAM CARD) or a RAM card of 1MB or greater which is listed on the ZR-5700/5800 PCMCIA compatibility list

Operating procedure	Display
1) Enter the diagnostics. [ON + D + RESET]	Diagnostics menu display
2) Install a 1MB SRAM card.	
3) Press the MENU key once.	
4) Press the ▼ key six times. Select "No. 19 WRITE CHECK DATA to RAM CARD."	
5) Press the ENTER key.	** CHECK PCMCIA ** Check PCMCIA controller <<< CHECK OK!!>>>
6) Press the ENTER key.	** CHECK PCMCIA ** Write data to RAM CARD <<< CHECK OK!!>>>
7) Press the ON key, then press the MENU key once.	Diagnostics menu display
8) Press the ▼ key seven times. Select "No. 20 CHECK RAM CARD DATA (22)."	
9) Press the ENTER key.	** CHECK PCMCIA ** Check PCMCIA controller <<< CHECK OK!!>>>
10) Press the ENTER key.	** CHECK PCMCIA ** Checking RAM CARD data <<< CHECK OK!!>>>
11) Press the ON key.	Diagnostics menu display

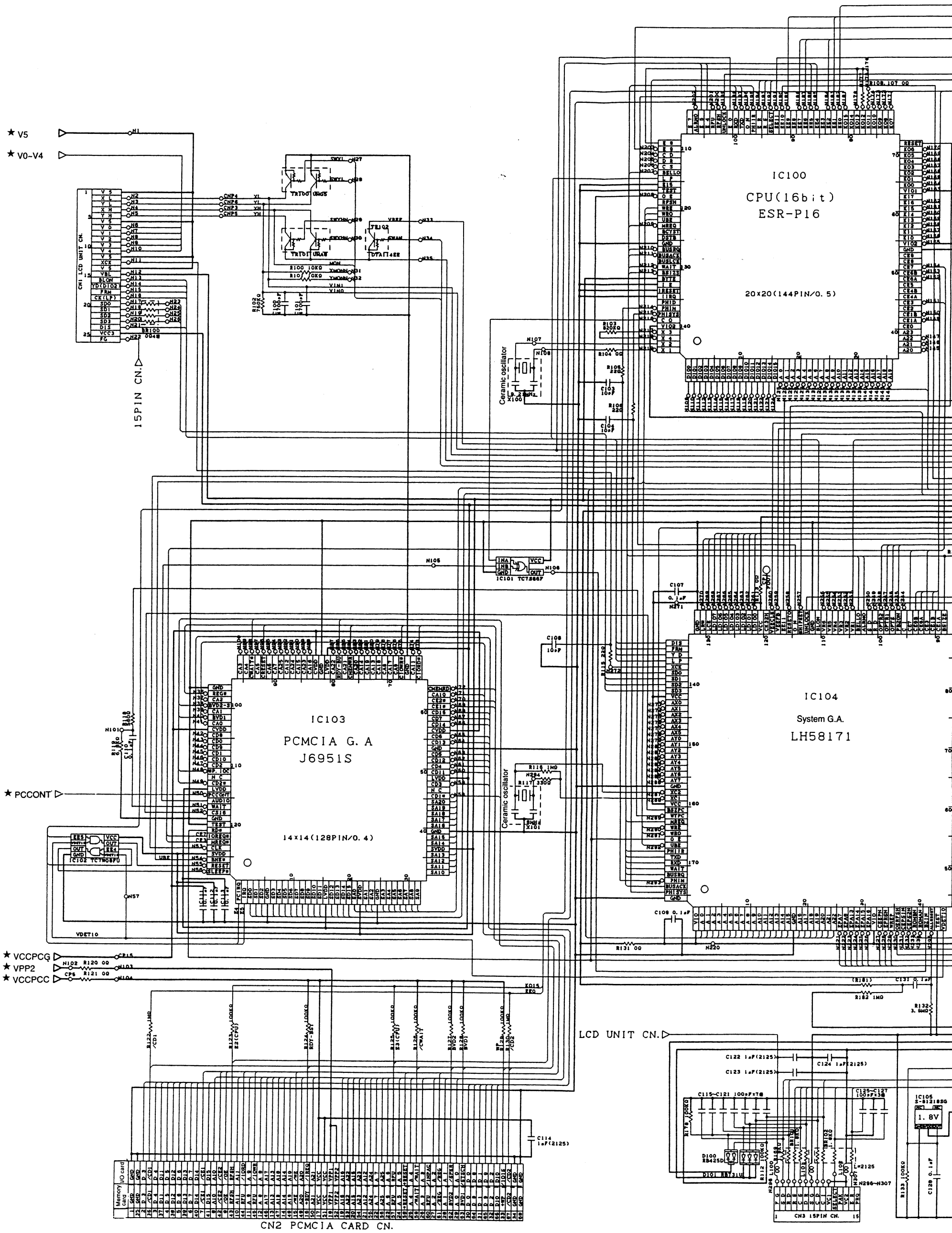
In 5), 6), 9), and 10), if <<CHECK OK!!>> is displayed, the set is normal.

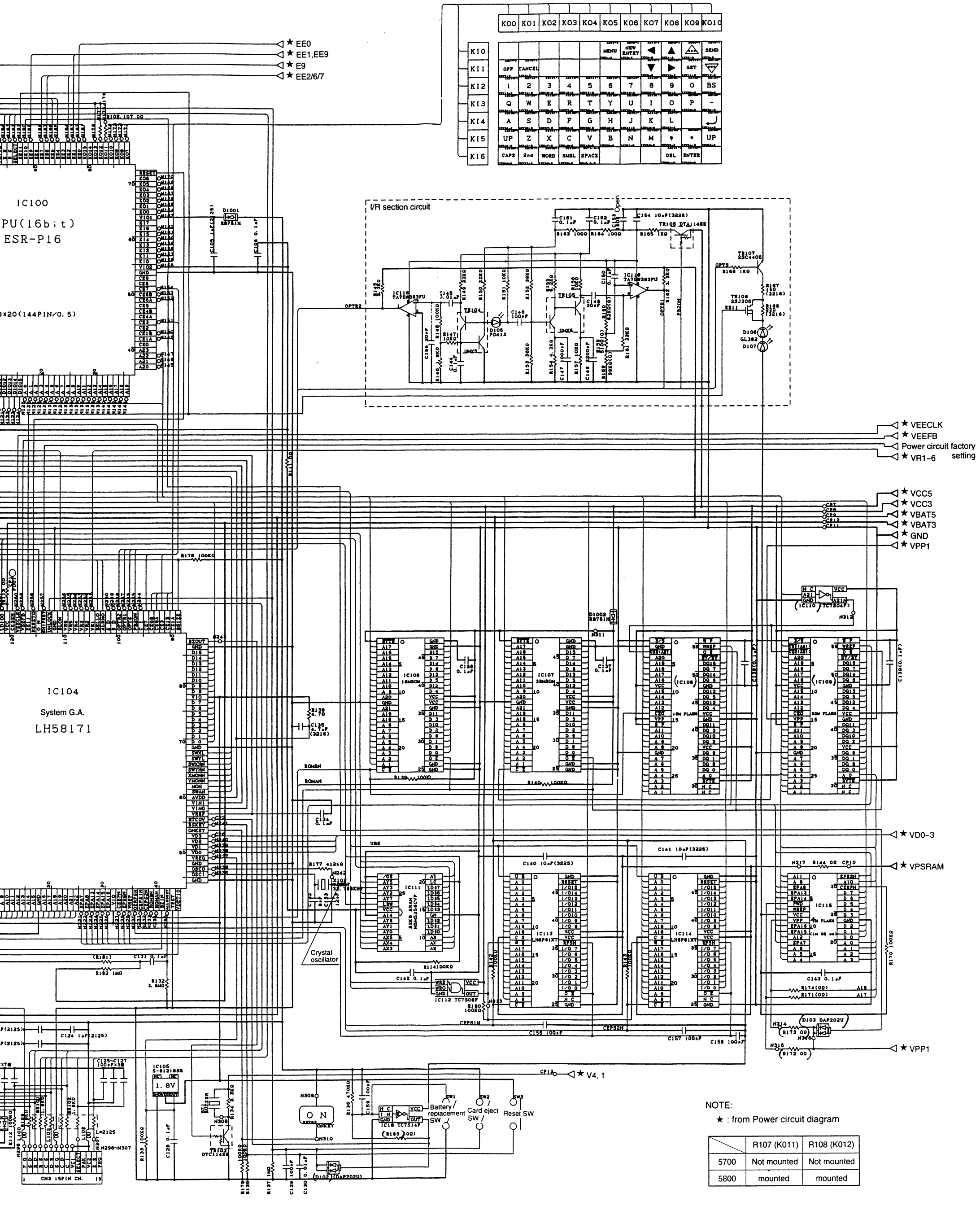
(Note) The write protect SW of the card must be released. (Not protected.)

(4) Perform procedure of No. 16 immediately after checking of No. 15 <<check OK>>. If not, an error may occur.

CHAPTER 6. CIRCUIT DIAGRAM & PARTS LAYOUT

(1) MAIN PWB-1. SYSTEM LOGIC CIRCUIT



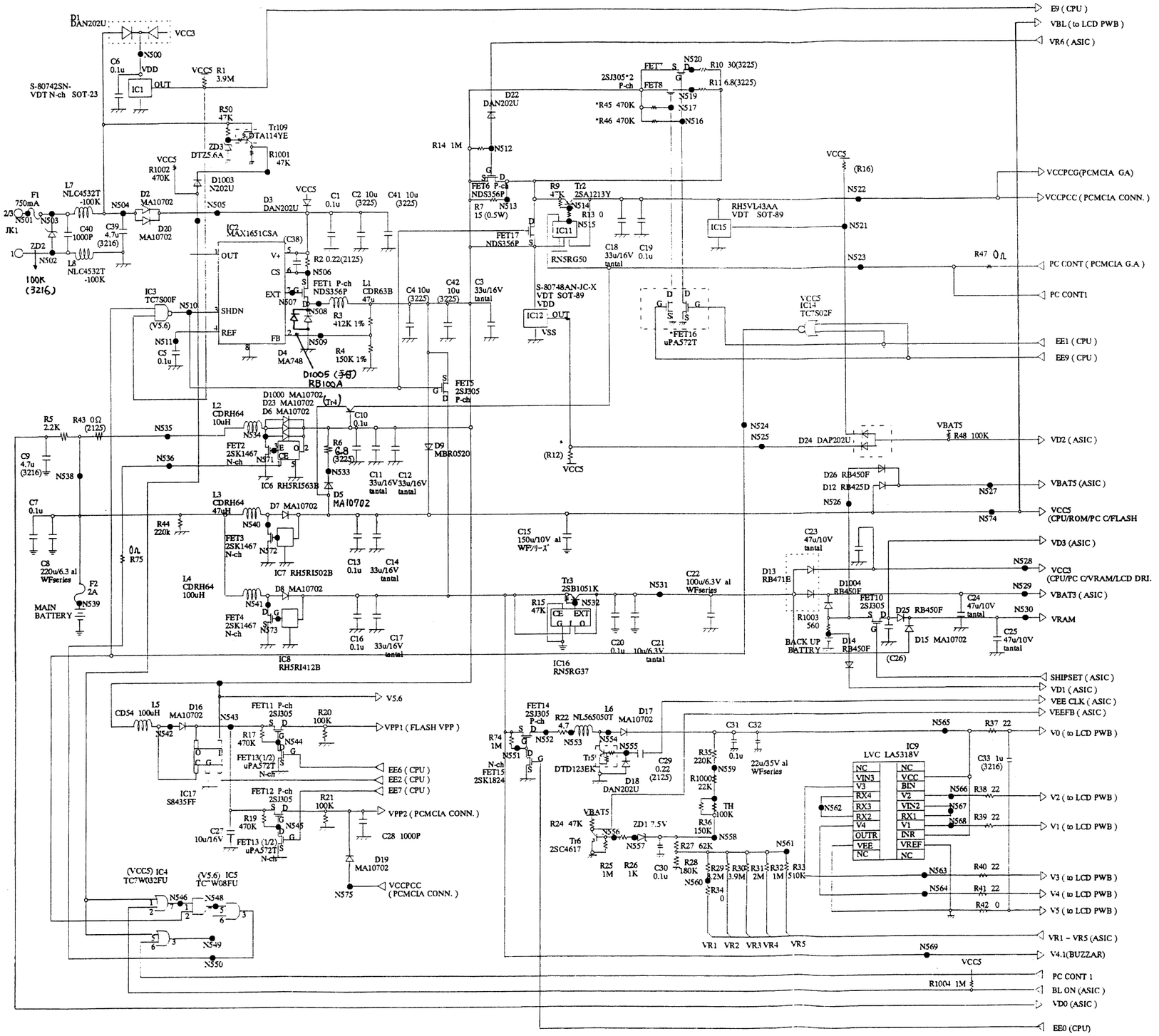


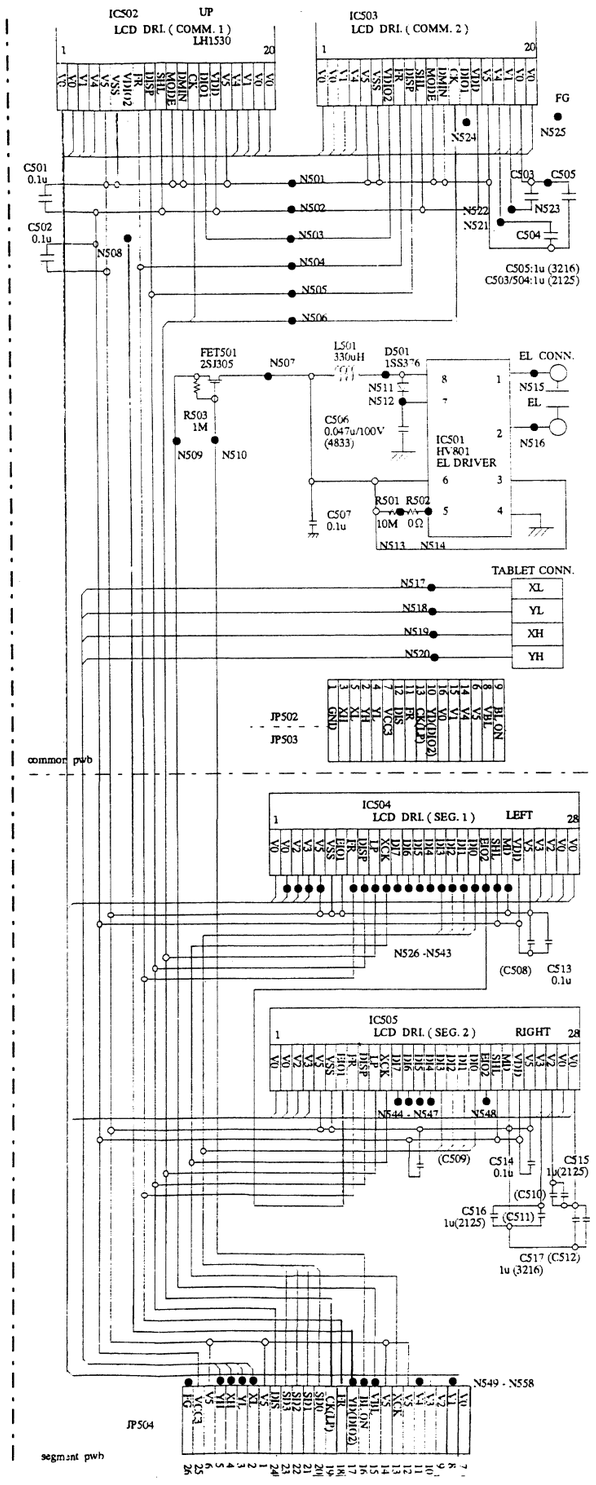
NOTE:

★ : from Power circuit diagram

	R107 (K011)	R108 (K012)
5700	Not mounted	Not mounted
5800	mounted	mounted

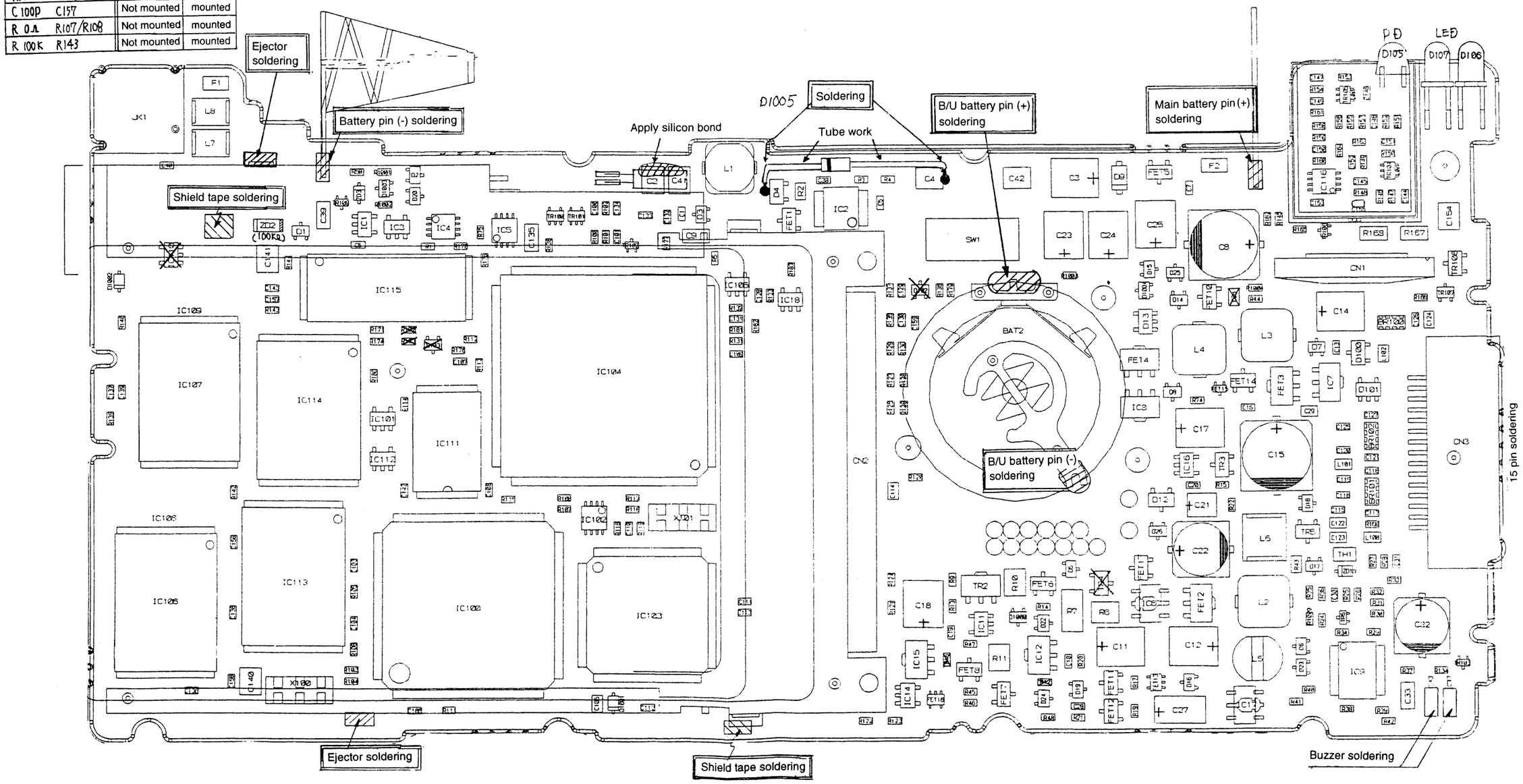
(2) MAIN PWB-2. POWER SUPPLY CIRCUIT



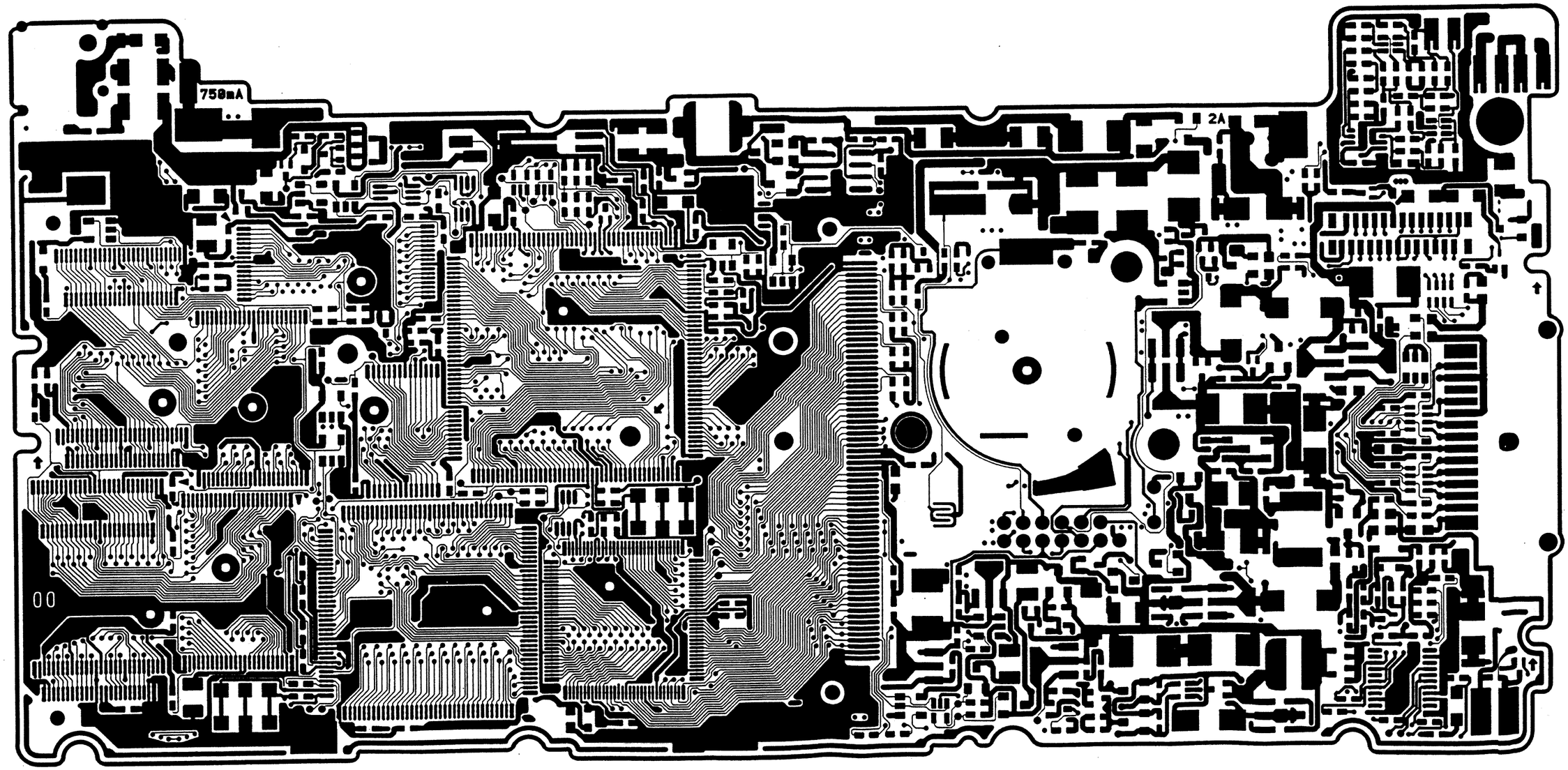


(3) MAIN PWB PARTS LAYOUT

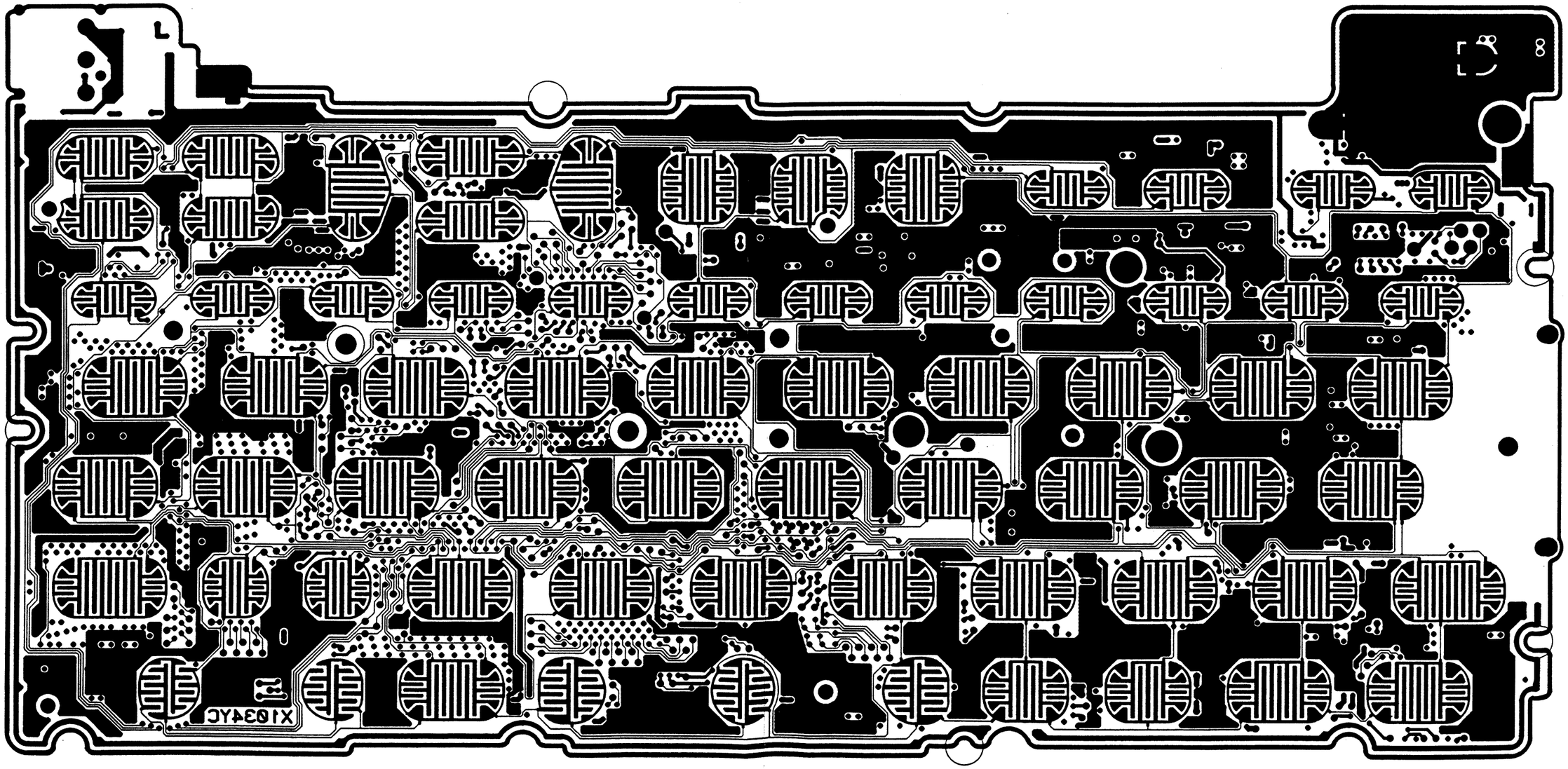
	5700	5800
RAM IC114	Not mounted	mounted
C100P C157	Not mounted	mounted
R 0Ω R107/R108	Not mounted	mounted
R 100K R143	Not mounted	mounted



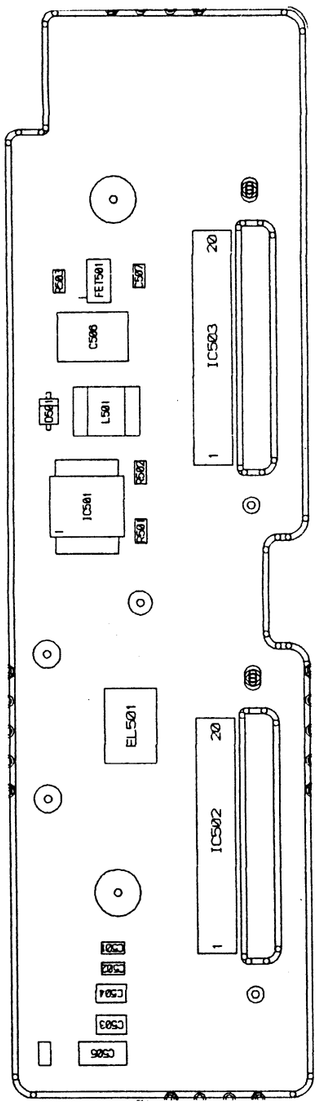
(4) MAIN PWB PATTERN (Parts side)

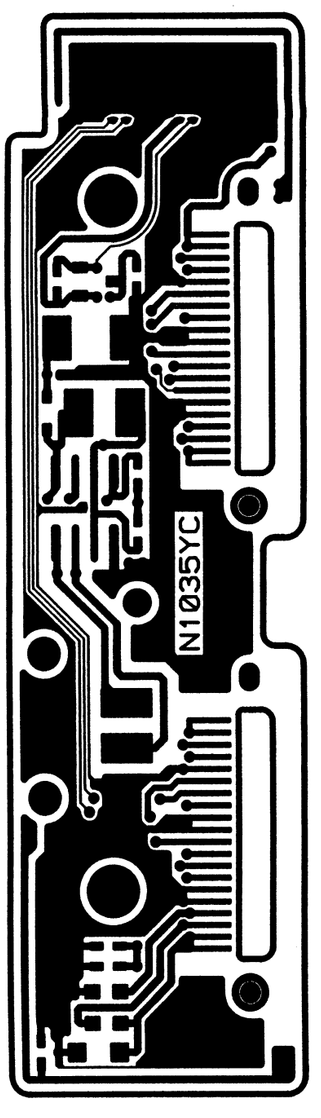


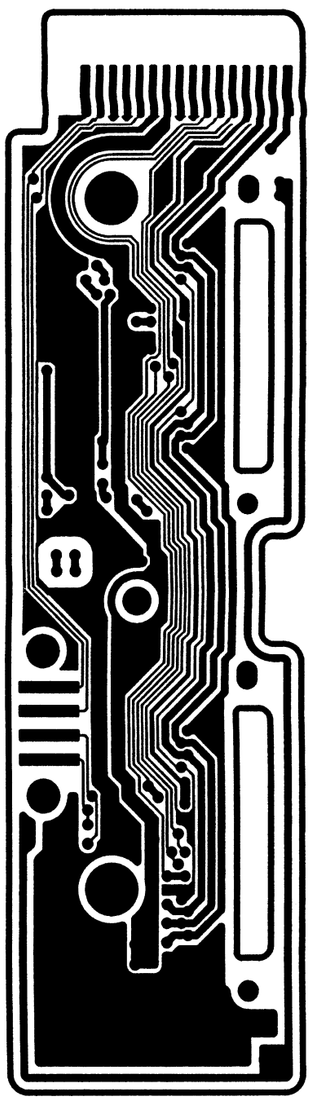
(5) MAIN PWB PATTERN (Key side)

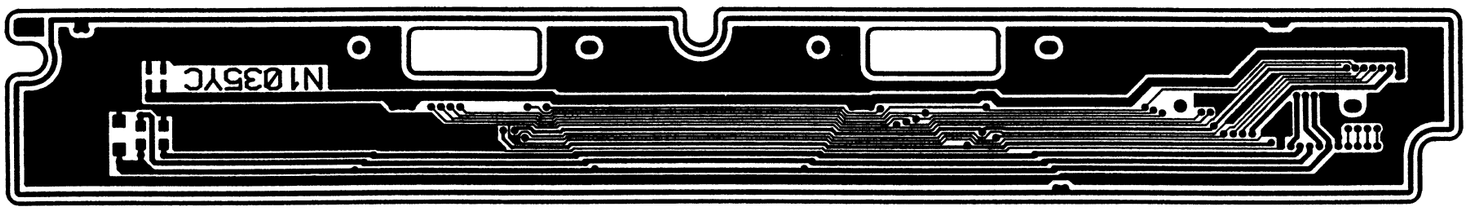


(7) Common PWB

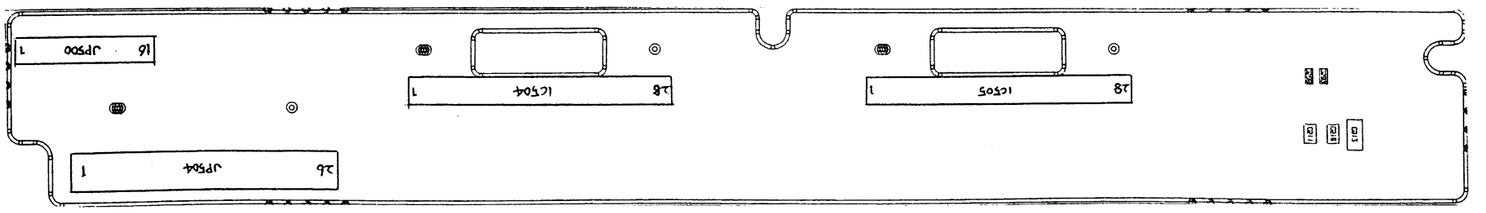






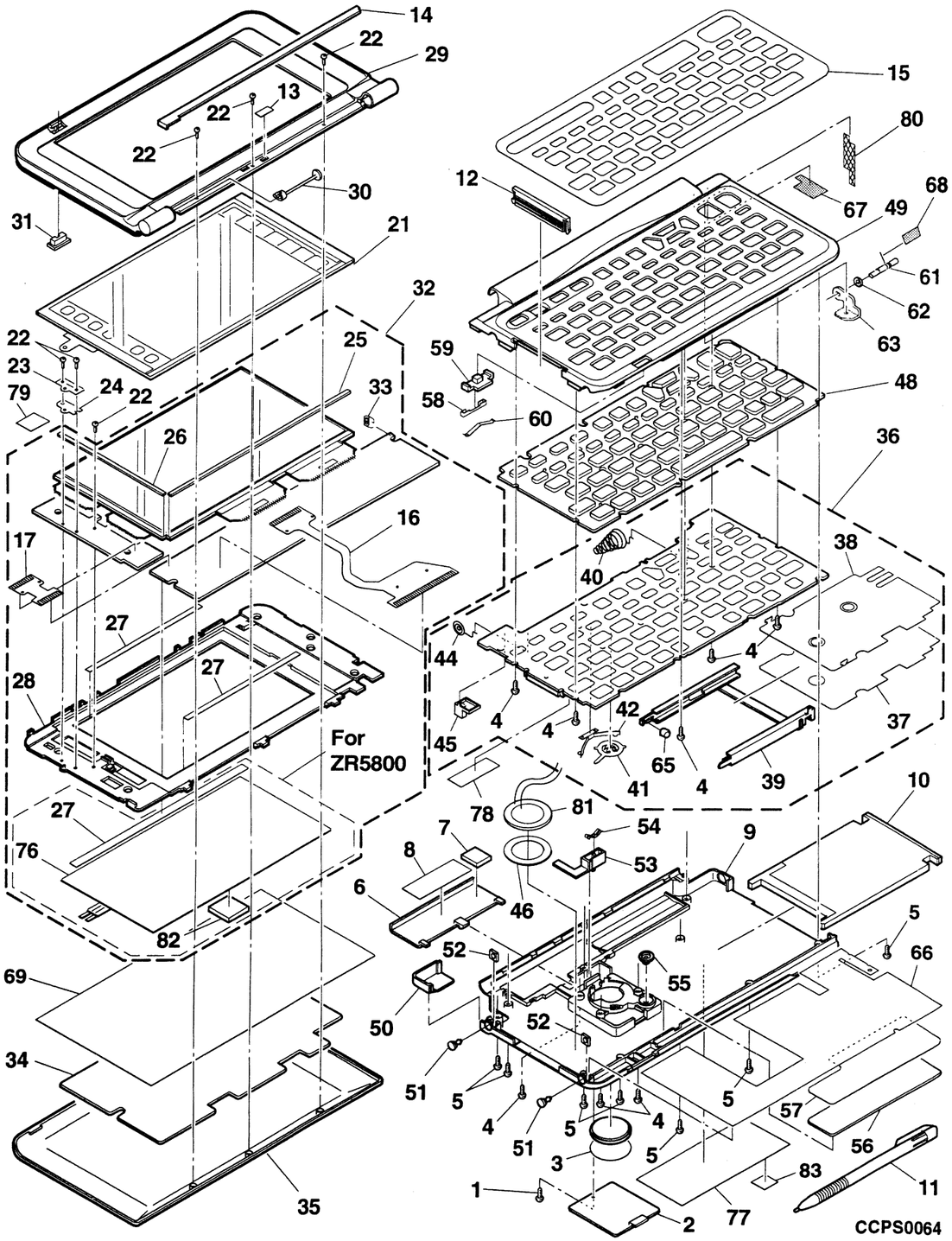


(6) Segment PWB



PARTS GUIDE

1 Exteriors



1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	ZR-5700	ZR-5800
1	LX-BZ1299CCZZ	AA		C	Screw (M1.7)	○	○
2	GFTAB1002YCZZ	AG		D	Battery cover B	○	○
3	PSPAP1404CCZZ	AA		C	Spacer(for back up battery)	○	○
4	LX-BZ1017PCZZ	AA		C	Screw A (M1.4)	○	○
5	LX-BZ1003PCZZ	AA		C	Screw (M1.7 L=5.6)	○	○
6	GFTAB1001YCZZ	AG		D	Battery cover A	○	○
7	PCUSS1003YCZZ	AB		C	Battery holding cushion	○	○
8	TLABZ1087PCZZ	AB		D	Battery caution label	○	○
9	GCABA1003YCA1	AQ		D	Key cabinet A	○	○
10	GiTA-1001YCZZ	AE		C	Dummy card	○	○
11	CPENP1004PCN1	AF		C	Pen unit	○	○
12	GFTAA1003YCZZ	AC		D	Connector cover (15pin)	○	○
13	PTPEH1005YCZZ	AA		D	Adhesive tape	○	○
14	LPLTP1001YCZZ	AE		C	Screw blind plate	○	○
15	PSHEZ1001YCA5	AN	N	D	Key deco.film	○	
	PSHEZ1001YCA6	AN	N	D	Key deco.film		○
16	QPWBM1037YCZZ	AL		C	FPC B	○	○
17	QPWBM1038YCZZ	AF		C	FPC A	○	○
21	CSW-Z1001YC04	BH		E	Tablet unit	○	
	CSW-Z1010YC01	BK		E	Tablet unit		○
22	LX-BZ1275CCZZ	AA		C	Screw (M1.7)	○	○
23	LANGK1002PCZZ	AB		C	Tablet angle B	○	○
24	PGUMM1003PCZZ	AB		C	Tablet rubber	○	○
25	PCUSS1001YCZZ	AA		C	Cushion A	○	○
26	PCUSS1002YCZZ	AA		C	Cushion B	○	○
27	PTPEH1013YCZZ	AB		D	LCD fixing tape	○	○
28	LHLDZ1009YCZZ	AH		C	LCD Holder	○	○
29	GCABB1002YCZ1	AH		D	Display cabinet B	○	○
30	LPiNS1001YCA1	AD		C	Hinge pin	○	○
31	PSPAZ1005YCZ1	AC		C	Cover lock spacer	○	○
32	DUNTL1187YCZZ	BT		E	LCD unit (include No.16–20,27,28)	○	
	DUNTL1198YCZZ	BU		E	LCD unit (include No.16–20,27,28,76)		○
33	MSPRC1006YCZZ	AB		C	Electrostatic spring	○	○
34	LPLTP1002YCZZ	AK		C	Reinforce plate	○	○
35	GCABA1001YCZ3	AS		D	Display cabinet A	○	
	GCABA1001YCZ4	AS		D	Display cabinet A		○
36	DUNTK1225YCZS	CG	N	E	PWB unit (include No.37–42,44,45,65)[Canada]	○	
	DUNTK1219YCZS	CL	N	E	PWB unit (include No.37–42,44,45,65)[Canada]		○
	DUNTK1229YCZS	CK	N	E	Main PWB unit (include No.37–42,44,45,65)[except Canada]	○	
	DUNTK1233YCZS	CN	N	E	Main PWB unit (include No.37–42,44,45,65)[except Canada]		○
37	PSHEZ1008YCZZ	AD		C	PWB blind sheet	○	○
38	PSHEZ1004YCZZ	AF		C	Electrostatic sheet	○	○
39	KMEC-1003PCA2	AS		C	Ejector	○	○
40	QTANB1002YCZZ	AB		C	Battery terminal(main) ⊖	○	○
41	QTANZ1604CCZZ	AC		C	Battery terminal(back up) ⊖		
42	QTANZ1598CCZZ	AB		C	Battery terminal(back up) ⊕	○	○
44	QTANB1001YCZZ	AB		C	Battery terminal(main) ⊕	○	○
45	PSLDP1002YCZZ	AC		C	Shield plate	○	○
46	PTPEH1508CC01	AB		D	Buzzer tape	○	○
48	PGUMM1001YCZ3	AX		C	Key rubber	○	○
49	GCABB1004YCZ5	AM		D	Key cabinet B	○	
	GCABB1004YCZ7	AM	N	D	Key cabinet B		○
50	PFiLW1001YCZZ	AD		D	IR filter	○	○
51	PGUMM1691CCZZ	AA		C	Rubber cap	○	○
52	LANGK1002YCZZ	AB		C	Modem angle	○	○
53	JKNBZ1002YCZZ	AD		C	Battery exchange knob	○	○
54	QCNTM1056CC02	AB		C	Contact	○	○
55	PGUMM1002PCZZ	AB		C	Reset rubber	○	○
56	PTPEH1003YCZZ	AB		D	Fixing tape	○	○
57	LPLTM1003YCZZ	AC		C	Reinforce plate	○	○
58	MSPRC1018PCZZ	AC		C	Cover lock spring	○	○
59	JKNBZ1001YCZZ	AC		C	Cover lock knob	○	○
60	MSPRP1010PCZZ	AC		C	Pop-up spring	○	○
61	MJNTP1001YCZZ	AP		C	Hinge unit	○	○
62	PSPAP1006YCZZ	AB		C	Hinge spacer	○	○
63	LANGK1001YCZZ	AC		C	Hinge angle	○	○
65	PTUB-1001YCZZ	AC		C	Insulate tube	○	○
66	PSLDC1007YCZZ	AG		C	Electrostatic sheet for key cabinet	○	○
67	PTPEH1006YCZZ	AD		D	Copper leaf tape A	○	○
68	PTPEH1007YCZZ	AB		D	Copper leaf tape B	○	○
69	PSLDC1009YCZZ	AF		C	Electrostatic sheet for display	○	○
76	RLMPL1003YCZZ	AZ		E	EL panel		○
77	TLABM1052YCZZ	AE	N	D	Name plate label	○	
	TLABM1055YCZZ	AE	N	D	Name plate label		○
78	PZETL1007YCZZ	AA		C	Insulate tape	○	○
79	PZETL1016YCZZ	AA	N	C	Insulate tape [except Canada]	○	○

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	ZR-5700	ZR-5800
80	PSLDC1009YCZZ	AF		C	Display electrostatic sheet	○	○
	PTPEH1017YCZZ	AB	N	D	Copper leaf tape C	○	○
81	RALMB1043CCZZ	AD		B	Alarm [BZ1]	○	○
82	PCUSS1014YCZZ	AB	N	C	EL cushion		○
83	TLABS1072YCZZ	AC	N	D	C-TICK label [Australia]	○	○

2 Packing material&Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	ZR-5700	ZR-5800
1	TiNSE1049YCZZ	AS	N	D	Instruction book (English) [Canada]	○	○
	TiNSF1050YCZZ	AU	N	D	Instruction book (French) [Canada]	○	○
	TiNSK1052YCZZ	AS	N	D	Instruction book (Pager) [Canada]	○	○
	TiNSE1049YC01	AS	N	D	Instruction book (English) [except Canada]	○	○
3	SPAK-547ECCZZ	AB		D	Vinyl bag (125 × 280mm) (for set)	○	○
4	SPAKA1160YCZZ	AF	N	D	Packing cushion for set [Canada]	○	○
	SPAKA1158YCZZ	AD		D	Packing cushion for set [except Canada]	○	○
5	SPAKA1151YCZZ	AD	N	D	Packing cushion for battery [Canada]	○	○
	SPAKA1164YCZZ	AE	N	D	Packing cushion for battery [except Canada]	○	○
6	SPAKC1155YCZZ	AK	N	D	Packing case [Canada]	○	
	SPAKC1152YCZZ	AK	N	D	Packing case [Canada]		○
	SPAKC1165YCZZ	AK	N	D	Packing case [Other countries]	○	
	SPAKC1161YCZZ	AK	N	D	Packing case [Germany]	○	
	SPAKC1169YCZZ	AK	N	D	Packing case [Other countries]		○
	SPAKC1166YCZZ	AK	N	D	Packing case [Germany]		○
7	SSAKAQ014YDEÖ	AA		D	Vinly bag (0.03t × 50 × 80) (for battery)	○	○
12	TCADU1044PCZZ	AA		D	Caution card	○	○
13	TiNSE1070YCZZ	AQ	N	D	Instruction book (Supplement)	○	○
	TiNSF1051YCZZ	AR	N	D	Instruction book (French) (Supplement)	○	○
14	TGANE1002CS02	AB		D	Warraty card [Canada]	○	○
	TGANE1003CSZZ	AD		D	Warranty card [EU]	○	○
	TGANE1114CCN1	AB		D	Warranty card [Australia]	○	○
17	TCADU1019YCZZ	AC		D	User card [Canada]	○	○
	TCADU1052YCZZ	AC	N	D	User card [except Canada]	○	○
18	TCADZ1050YCZZ	AC	N	D	Battery explanatory card [Canada]	○	○
19	TCADZ1051YCZZ	AC	N	D	Battery card [Canada]	○	○
20	TLABS1034YCZZ	AD		D	Noise label [Canada]	○	○

3 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	ZR-5700	ZR-5800
1	KMEC-1003PCA2	AS		C	Ejector	○	○
2	PSHEZ1004YCZZ	AF		C	Electrostatic sheet	○	○
3	PSHEZ1008YCZZ	AD		C	PWB blind sheet	○	○
4	PSLDP1002YCZZ	AC		C	Shield plate	○	○
6	PTUB-1001YCZZ	AC		C	Insulate tube	○	○
8	QCNCM1015PC68	AS		C	Connector (68pin) [CN2]	○	○
9	QCNCW1014YC26	AG		C	Connector (26pin) [CN1]	○	○
10	QCNCW1018PC15	AN		C	Connector (15pin) [CN3]	○	○
⚠ 11	QFS-L1005PCZZ	AF		A	Fuse (750mA) [F1]	○	○
⚠ 12	QFS-L9312QCZZ	AF		A	Fuse (2A) [F2]	○	○
13	QJAKE1001PCZZ	AE		C	Adaptor jack (2pin)	○	○
14	QTANB1001YCZZ	AB		C	Battery terminal(main) ⊕	○	○
15	QTANB1002YCZZ	AB		C	Battery terminal(main) ⊖	○	○
16	QTANZ1598CCZZ	AB		C	Battery terminal(back up) ⊕	○	○
17	QTANZ1604CCZZ	AC		C	Battery terminal(back up) ⊖	○	○
19	RC-CZ1067RC1C	AE		C	Capacitor (16WV 10μF) [C4,42,140,141,154](Canada only)	○	○
	RC-CZ1067RC1C	AE		C	Capacitor (16WV 10μF) [C140,141,154](except Canada)	○	○
20	RC-CZ4750RC1C	AD		C	Capacitor (16WV 4.7μF) [C9,39,135]	○	○
21	RC-KY1051RC1E	AC		C	Capacitor (25WV 1.0μF) [C33]	○	○
22	RC-SZ1061RC1C	AF		C	Capacitor (16WV 10μF) [C27](Canada only)	○	○
	RC-SZ1061RC1C	AF		C	Capacitor (16WV 10μF) [C4,27](except Canada)	○	○
23	RC-SZ1063RC0J	AF		C	Capacitor (6.3WV 10μF) [C21]	○	○
24	RC-SZ3364RC1C	AH		C	Capacitor (16WV 33μF) [C3,11,12,14,17,18]	○	○
25	RC-SZ4760RC1A	AH		C	Capacitor (10WV 47μF) [C23,24,25]	○	○
26	RCiLZ1011YCZZ	AE		C	Coil (1.8mH) [L6]	○	○
27	RCiLZ1012PCZZ	AC		C	Chip coil [L100,101,102](Canada only)	○	○
	RCiLZ1012PCZZ	AC		C	Chip coil [L101,102](except Canada)	○	○
28	RCiLZ1018YCZZ	AE		C	Coil (NLC45-100K) [L7,8](Canada only)	○	○
29	RCiLZ1024YCZZ	AF		C	Coil (CDR56B 47μH) [L1](Canada only)	○	○
30	RCiLZ1025YCZZ	AF		C	Coil (CDRH64 100μH) [L4]	○	○
31	RCiLZ1027YCZZ	AF		C	Coil (CDRH64 10μH) [L2]	○	○
32	RCiLZ1028YCZZ	AF		C	Coil (CDRH64 47μH) [L3]	○	○

3 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION		ZR-5700	ZR-5800
33	RCiLZ2363RCZZ	AF		C	Coil (CD54 100μH)	[L5]	○	○
34	RCRMC1001YCZZ	AE		B	Crystal (9.21MHz)	[X100]	○	○
35	RCRMC1007YCZZ	AF		B	Crystal (8MHz)	[X101]	○	○
36	RCRSP1007YCZZ	AE	N	B	Crystal (26MHz)	[X102]	○	○
37	RMPTQ4000QCJJ	AB		B	Block resistor (0Ω × 4)	[BR100](Canada only)	○	○
	RMPTQ4221QCJJ	AC		B	Block resistor (220Ω × 4)	[BR100](except Canada)	○	○
38	RMPTQ4182QCJJ	AC		B	Block resistor (1.8KΩ × 4)	[BR101,102]	○	○
39	VCCCCY1HH100D	AA		C	Capacitor (50WV 10pF)	[C103,104,108](Canada only)	○	○
	VCCCCY1HH100D	AA		C	Capacitor (50WV 10pF)	[C103,104,108,160,161,162,163](except Canada)	○	○
40	VCCCCY1HH101J	AA		C	Capacitor (50WV 100pF)	[C115,116,117,118,119,120,121,125,126,127,129,146,156,158,159](Canada only)	○	
	VCCCCY1HH101J	AA		C	Capacitor (50WV 100pF)	[C126,129,146,156,158,159](except Canada)	○	
	VCCCCY1HH101J	AA		C	Capacitor (50WV 100pF)	[C115,116,117,118,119,120,121,125,126,127,129,146,156,157,158,159](Canada only)		○
	VCCCCY1HH101J	AA		C	Capacitor (50WV 100pF)	[C126,127,146,156,157,158,159](except Canada)		○
41	VCCCCY1HH120J	AA		C	Capacitor (50WV 12pF)	[C133]	○	○
42	VCCCCY1HH200J	AA		C	Capacitor (50WV 20pF)	[C149,155](Canada only)	○	○
	VCCCCY1HH200J	AA		C	Capacitor (50WV 20pF)	[C115,116,117,118,119,120,121,125,127,149,155](except Canada)	○	○
43	VCCCCY1HH8R0D	AA		C	Capacitor (50WV 8.0pF)	[C132]	○	○
44	VCEAPL0JN107M	AF		C	Capacitor (4.3WV 100μF)	[C22]	○	○
45	VCEAPL0JN227M	AF		C	Capacitor (4.3WV 220μF)	[C8]	○	○
46	VCEAPL1AN157M	AF		C	Capacitor (10WV 150μF)	[C15]	○	○
47	VCEAPL1VN226M	AF		C	Capacitor (35WV 22μF)	[C32]	○	○
48	VCKYCY1EF103Z	AA		C	Capacitor (25WV 0.010μF)	[C130,145]	○	○
49	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C1,5,6,7,10,13,16,19,20,30,31,106,107,109,110](Canada only)	○	○
	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C111,112,113,128,131,134,136,137,142,143,144,150,151,152](Canada only)	○	○
	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C1,5,6,7,10,13,16,19,20,30,31,106,107,110](except Canada)	○	○
	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C111,112,113,128,131,134,136,142,143,144,150,151,152](except Canada)	○	○
50	VCKYCY1HB102K	AA		C	Capacitor (50WV 1000PF)	[C28,40,147]	○	○
51	VCKYCY1HF222Z	AA		C	Capacitor (50WV 2200PF)	[C148]	○	○
52	VCKYCY1HF472Z	AA		C	Capacitor (50WV 4700pF)	[C100,101]	○	○
53	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1.0μF)	[C105,114,122,123,124](Canada only)	○	○
	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1.0μF)	[C114,122,123,124](except Canada)	○	○
54	VCKYTV1EF224Z	AB		C	Capacitor (25WV 0.22μF)	[C29]	○	○
55	VHDDAN202U/-1	AB		B	Diode (DAN202U)	[D1,3,18,22,1003](Canada only)	○	○
	VHDDAN202U/-1	AB		B	Diode (DAN202U)	[D1,3,18,22,1003,1006](except Canada)	○	○
56	VHDDAP202U/-1	AB		B	Diode (DAP202U)	[D24](Canada only)	○	○
	VHDDAP202U/-1	AB		B	Diode (DAP202U)	[D24,103](except Canada)	○	○
57	VHDMA748///-1	AD		B	Diode (MA748)	[D4](Canada only)	○	○
	VHDRB160L40-1	AD		B	Diode (RB160L40)	[D4](except Canada)	○	○
58	VHDMBR0520LT1	AE		B	Diode (MBR0520LT1)	[D9]	○	○
59	VHDRB425D//-1	AE		B	Diode (RB425D)	[D12,100]	○	○
60	VHDRB450F//-1	AD		B	Diode (RB450F)	[D14,25,26,1004]	○	○
61	VHDRB471E//-1	AE		B	Diode (RB471E)	[D13](Cnada only)	○	○
62	VHDRB731U//-1	AE		B	Diode (RB731U)	[D101]	○	○
63	VHDRB751H//-1	AD		B	Diode (RB751H)	[D1001,1002]	○	○
64	VHEDTZ5.6A/-1	AC		B	Zener diode (DTZ751H)	[ZD3]	○	○
65	VHEUDZ7.5B/-1	AC		B	Zener diode (UDZ7.5B)	[ZD1]	○	○
66	VHH104HT///-1	AF		B	Thermistor (68K)	[TH1]	○	○
67	VHiJ6951SA/-1	AZ		B	IC (J6951SA)	[IC103]	○	○
68	VHiLA5318V/-1	AM		B	IC (LA5318V)	[IC9]	○	○
69	VHiLH535DT7-1	BG	N	B	IC (LH535DT7)	[IC107](Canada)	○	○
	VHiLH535DTC-1	BG	N	B	IC (LH535DTC)	[IC107](except Canada)	○	○
70	VHiLH537DYE-1	BB		B	IC (LH537DYE)	[IC106](Canada)	○	○
	VHiLH537DV1-1	BB	N	B	IC (LH537DV1)	[IC106](except Canada)	○	○
71	VHiLH5809//-1	BF		B	IC (LH5809)	[IC100]	○	○
72	VHiLH58171/-1	BE		B	IC (LH58171)	[IC104]	○	○
73	VHiLH6P82T/-1	BQ		B	IC (LH6P82T)	[IC113]	○	
	VHiLH6P82T/-1	BQ		B	IC (LH6P82T)	[IC113,114]		○
74	VHiMAX1651/-1	AS		B	IC (MAX1651)	[IC2]	○	○
75	VHiM5256CVP-1	AX		B	IC (M5256CVP)	[IC111]	○	○
76	VHiRH5Ri412-1	AH		B	IC (RH5RI412)	[IC8]	○	○
77	VHiRH5Ri502B1	AH		B	IC (RH5RI502B1)	[IC7]	○	○
78	VHiRH5Ri563B1	AL		B	IC (RH5RI563B1)	[IC6]	○	○
79	VHiRH5VL43AA1	AE		B	IC (RH5VL43AA1)	[IC15]	○	○
80	VHiRN5RG37A-1	AG		B	IC (RN5RG37A)	[IC16]	○	○
81	VHiRN5RG50/-1	AF		B	IC (RN5RG50)	[IC11]	○	○
82	VHiS80742SND6	AF		B	IC (S80742SND6)	[IC1]	○	○
83	VHiS80748ANJC	AE		B	IC (S80748ANJC)	[IC12]	○	○
84	VHiS81218SG-1	AF		B	IC (S81218SG)	[IC105]	○	○
85	VHiS8435FF/-1	AH		B	IC (S8435FF)	[IC17]	○	○
86	VHiTC7S00F/-1	AC		B	IC (TC7S00F)	[IC3]	○	○
87	VHiTC7S02F/-1	AC		B	IC (TC7S02F)	[IC14]	○	○
88	VHiTC7S08F/-1	AC		B	IC (TC7S08F)	[IC112]	○	○
89	VHiTC7S14F/-1	AD		B	IC (TC7S14F)	[IC18]	○	○

3 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	ZR-5700	ZR-5800
90	VHiTC7S86F/-1	AD		B	IC (TC7S86F) [IC101]	○	○
91	VHiTC7W08FU-1	AE		B	IC (TC7W08FU) [IC5,102]	○	○
92	VHiTC7W32FU//	AE		B	IC (TC7W32FU) [IC4]	○	○
93	VHi29F040A-12	BF		B	IC (29F040A-12) [IC115](Canada only)	○	○
	VHiF001BXT120	BA		B	IC (F001BXT120) [IC115](except Canada)	○	○
94	VHi75W393FU-1	AE		B	IC (75W393FU) [IC116]	○	○
95	VHMA10702//-1	AC		B	Diode (MA10702) [D2,6,7,8,15,16,17,19,20,23,1000,5]	○	○
96	VHPGL382M//-1	AH		B	LED (PGL382M) [D106,107]	○	○
97	VHPPD413Pi1-1	AE		B	Photo transistor (PD413PI1) [D105]	○	○
98	VRS-CY1JD000J	AA		C	Resistor (0.063W 0Ω ±5%) [R13,34,42,47,75,104,111,113,120,121,131,144,171,174,1003]	○	
	VRS-CY1JD000J	AA		C	Resistor (0.063W 0Ω ±5%) [R13,34,42,47,75,104,107,108,111,113,120,121,131,144,171,174,1003]		○
99	VRS-CY1JD101J	AA		C	Resistor (1/16W 100Ω ±5%) [R163,164]	○	○
100	VRS-CY1JD102J	AA		C	Resistor (0.063W 1.0KΩ ±5%) [R26,165,166]	○	○
101	VRS-CY1JD103J	AA		C	Resistor (1/16W 10KΩ ±5%) [R100,101,147,151,156,157]	○	○
102	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%) [R20,21,48,112,114,123,124,125,126,127,128,129]	○	
	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%) [R135,139,140,142,148,170,176,178,179,180]	○	
	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%) [R20,21,48,112,114,123,124,125,126,127,128,129]		○
	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%) [R135,139,140,142,143,148,170,176,178,179,180]		○
103	VRS-CY1JD105J	AA		C	Resistor (1/16W 1.0MΩ ±5%) [R14,25,32,74,116,122,130,133,137,182,1004] (Canada only)	○	
	VRS-CY1JD105J	AA		C	Resistor (1/16W 1.0MΩ ±5%) [R14,25,32,74,116,122,130,137,182,1004] (except Canada)	○	
104	VRS-CY1JD154F	AA		C	Resistor (1/16W 150KΩ ±1%) [R4]	○	○
105	VRS-CY1JD154J	AA		C	Resistor (1/16W 150KΩ ±5%) [R36]	○	○
106	VRS-CY1JD182J	AA		C	Resistor (0.063W 1.8KΩ ±5%) [R146,169]	○	○
107	VRS-CY1JD184J	AA		C	Resistor (1/16W 180KΩ ±5%) [R28]	○	○
108	VRS-CY1JD205J	AA		C	Resistor (1/16W 2.0MΩ ±5%) [R31]	○	○
109	VRS-CY1JD220J	AA		C	Resistor (1/16W 22Ω ±5%) [R37,38,39,40,41,105,106,115]	○	○
110	VRS-CY1JD222J	AA		C	Resistor (1/16W 2.2KΩ ±5%) [R5]	○	○
111	VRS-CY1JD223J	AA		C	Resistor (1/16W 22KΩ ±5%) [R150,1000]	○	○
112	VRS-CY1JD224J	AA		C	Resistor (1/16W 220KΩ ±5%) [R35,44]	○	○
113	VRS-CY1JD331J	AA		C	Resistor (1/16W 330Ω ±5%) [R117]	○	○
114	VRS-CY1JD332J	AA		C	Resistor (1/16W 3.3KΩ ±5%) [R134,145,162]	○	○
115	VRS-CY1JD333J	AA		C	Resistor (1/16W 33KΩ ±5%) [R149,161]	○	○
116	VRS-CY1JD363J	AA		C	Resistor (1/16W 36KΩ ±5%) [R153]	○	○
117	VRS-CY1JD393G	AA		C	Resistor (0.063W 39KΩ ±2%) [R158]	○	○
118	VRS-CY1JD393J	AA		C	Resistor (1/16W 39KΩ ±5%) [R152]	○	○
119	VRS-CY1JD395J	AA		C	Resistor (0.063W 3.9MΩ ±5%) [R1,30,132]	○	○
120	VRS-CY1JD4R7J	AA		C	Resistor (0.063W 4.7Ω ±5%) [R22,138]	○	○
121	VRS-CY1JD432J	AA		C	Resistor (0.063W 4.3KΩ ±5%) [R154]	○	○
122	VRS-CY1JD473J	AA		C	Resistor (0.063W 47KΩ ±5%) [R9,15,24,50,1001]	○	○
123	VRS-CY1JD474J	AA		C	Resistor (1/16W 470KΩ ±5%) [R17,19,45,46,136,1002]	○	○
124	VRS-CY1JD511G	AA		C	Resistor (0.063W 510Ω ±2%) [R159]	○	○
125	VRS-CY1JD514J	AA		C	Resistor (1/16W 510KΩ ±5%) [R33]	○	○
126	VRS-CY1JD561J	AA		C	Resistor (1/16W 560Ω ±5%) [R118]	○	○
127	VRS-CY1JD622J	AA		C	Resistor (1/16W 6.2KΩ ±5%) [R155]	○	○
128	VRS-CY1JD623G	AA		C	Resistor (0.063W 62KΩ ±2%) [R160]	○	○
129	VRS-CY1JD623J	AA		C	Resistor (1/16W 62KΩ ±5%) [R27]	○	○
130	VRS-CY1JD682J	AA		C	Resistor (1/16W 6.8KΩ ±5%) [R119]	○	○
131	VRS-CY1JD754J	AA		C	Resistor (0.063W 750KΩ ±5%) [R102](Canda only)	○	○
	VRS-CY1JD754J	AA		C	Resistor (0.063W 750KΩ ±5%) [R102,133](except Canada)	○	○
132	VRS-CY1JD824J	AA		C	Resistor (0.063W 820KΩ ±5%) [R103]	○	○
133	VRS-CY1JD825J	AA		C	Resistor (0.063W 8.2MΩ ±5%) [R29]	○	○
134	VRS-TP2BD104J	AA		C	Resistor (1/4W 10KΩ ±5%) [ZD2]	○	○
135	VRS-TP2BD150J	AA		C	Resistor (1/8W 15Ω ±5%) [R167]	○	○
136	VRS-TP2BD220J	AA		C	Resistor (1/8W 22Ω ±5%) [R168]	○	○
137	VRS-TS2BTR22F	AC		C	Resistor (1/8W 0.22Ω ±1%) [R2]	○	○
138	VRS-TW2ED300J	AB		C	Resistor (1/4W 30Ω ±5%) [R10]	○	○
139	VRS-TW2ED6R8J	AB		C	Resistor (1/4W 6.8Ω ±5%) [R6,11]	○	○
140	VRS-TX2HD150J	AB		C	Resistor (1/2W 15Ω ±5%) [R7]	○	○
141	VRSCY1JD4123F	AA		C	Resistor (1/16W 412KΩ ±1%) [R3,177]	○	○
142	VSDTA114EE/-1	AC		B	Transistor (DTA114EE) [TR102,106]	○	○
143	VSDTA114YE/-1	AC		B	Transistor (DTA114YE) [TR109]	○	○
144	VSDTC114EE/-1	AC		B	Transistor (DRC114EE) [TR103]	○	○
145	VSDTD123EK/-1	AD		B	Transistor (DTD123EK) [TR5]	○	○
146	VSNDS356P//-1	AF		B	Transistor (NDS356P) [FET1,6,17](Cnada only)	○	○
	VSNDS356P//-1	AF		B	Transistor (NDS356P) [FET1,5,6,17](except Canada)	○	○
147	VSUMA8N////-1	AD		B	Transisor (UMA8N) [TR101]	○	○
148	VSUMG5N////-1	AD		B	Transistor (UMG5N) [TR100]	○	○
149	VSUMX5N////-1	AD		B	Transistor (SUMX5N) [TR104,105]	○	○
150	VSUPA572T//-1	AC		B	Transistor (UPA572T) [FET13,16]	○	○
151	VS2SA1213Y/-1	AC		B	Transistor (2SA1213Y) [TR2]	○	○
152	VS2SB1051KS-1	AC		B	Transistor (2SB1051KS) [TR3]	○	○
153	VS2SC4405-/-1	AD		B	Transistor (2SC4405) [TR107]	○	○
154	VS2SC4617-/-1	AC		B	Transistor (2SC4617) [TR6]	○	○

3 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION		ZR-5700	ZR-5800
155	VS2SJ305///-1	AE		B	Transistor (2SJ305)	[FET5,7,8,10,11,12,14,TR108]	○	○
156	VS2SK1467//-1	AE		B	Transistor (2SK1467)	[FET2,3,4]	○	○
157	VS2SK1824//-1	AB		B	Transistor (2SK1824)	[FET15]	○	○
158	VRS-TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%)	[R43]	○	○
160	RC-SZ4751RC1C	AE	N	C	Capacitor (16WV 4.7μF)	[C2,41]	○	○
161	RCiLZ1031YCZZ	AF	N	C	Coil (2pin)	[L1](except Canada)	○	○
162	RCiLZ1032YCZZ	AE	N	C	Coil (MZA102B)	[L103](except Canada)	○	○
163	RCiLZ1033YCZZ	AD	N	C	Coil (MMZ2012301B)	[L100](except Canada)	○	○
164	RCŌRF1005YCZZ	AE	N	C	Core (ACM4532-801)	[L7](except Canada)	○	○
	(Unit)							
901	DUNTK1225YCZS	CG	N	E	PWB unit	[Canada]	○	
	DUNTK1219YCZS	CL	N	E	PWB unit	[Canada]		○
	DUNTK1229YCZS	CK	N	E	Main PWB unit	[except Canada]	○	
	DUNTK1233YCZS	CN	N	E	Main PWB unit	[except Canada]		○

4 LCD PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION		ZR-5700	ZR-5800
1	RC-CZ1094CCZZ	AB		C	Capacitor (25WV 1.0μF)	[C505,517]	○	○
2	RCiLZ1029YCZZ	AE		C	Coil	[L501]		○
3	VCFRED2AD473J	AF		C	Capacitor (100WV 0.047μF)	[C506]		○
4	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C501,502,513,514]	○	
	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C501,502,507,513,514]		○
5	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1.0μF)	[C503,504,515,516]	○	○
6	VHDiSS376//-1	AD		B	Diode (ISS376)	[D501]		○
7	VHiHV801LG/-1	AM		B	IC (HV801LG)	[IC501]		○
8	VRS-CY1JD000J	AA		C	Resistor (0.063W 0Ω ±5%)	[R502]		○
9	VRS-CY1JD105J	AA		C	Resistor (1/16W 1.0MΩ ±5%)	[R503]	○	○
10	VRS-CY1JD106J	AA		C	Resistor (0.063W 10MΩ ±5%)	[R501]		○
11	VS2SJ305///-1	AE		B	Transistor (2SJ305)	[FET501]		○

SHARP

Date : Jul. 8, 1996

No. : PDA-038

INTELLIGENT TOOL : ZR-5000, ZR-5700, ZR-5800

Technical Report

V.1.0 1167
V.1.60 SI √

1.A CHANGE IN CUSHION MATERIAL FOR THE ZR-5000/5700/5800
2.DISCONTINUATION OF INCLUSION OF A SPARE BACKUP BATTERY (CR2032)
3.CHANGES TO THE PARTS OF THE ZR-5000/5700/5800

1. A change in cushion material for the ZR-5000/5700/5800

1-1.Model Name:

ZR-5000, ZR-5000I, ZR-5000G, ZR-5700, ZR-5800

1-2.General:

We had been intending to use the ZR-5000 set attachment cushion for new ZR-5800s. Recently, however, it was decided to make improvements, and the shape of the cushion for the ZR-5800 has been changed as a result.

(ZR-5000)

This models will use the aforementioned altered cushion from now on.

(ZR-5700/5800)

There are more operation manuals for the Canadian version of the ZR-5700/5800 than others, so further reinforcement have been required to the version and the newer cushion will be used.

1-3.Parts Changes:

Ref. No.	Model name	Version	P/G No.	Current parts	New parts		Parts name	Effective time	Interchangeability	Note
				Parts code	Parts code	Price rank				
1	ZR-5000	All	2 -4	SPAKA1030YCZZ	SPAKA1158YCZZ	AD	Packing cushion for set	Feb. '96	1	
	ZR-5000G	Germany								
	ZR-5000I	Italy								
	ZR-5700	Canada		SPAKA1158YCZZ	SPAKA1160YCZZ	AF			3	
	ZR-5800									

SHARP CORPORATION Personal Intelligent Systems Division

Deep yellow C

2. Discontinuation of inclusion of a spare backup battery (CR2032)

2-1.Model Name: ZR-5700, ZR-5800

2-2.General: A CR-2032 lithium battery has been pre-installed in the unit as a backup battery. However, this backup battery loses power gradually, even in storage. Therefore, to prepare for the results of long-term storage, an extra battery was packed with the units. We then learned that the battery does not lose significant amounts of power even when stored for long periods of time, so we have discontinued the inclusion of an extra backup battery in the packaging.

2-3.Parts Changes:

Ref. No.	Model name	Version	P/G No.	Current parts	New parts		Parts name	Effec-tive time	Inter-change-ability	Note
				Parts code	Parts code	Price rank				
2	ZR-5700 ZR-5800 ZR-5800FX	Canada U.S.A.	[2] -18	UBATZ6441CCMM	—	—	Backup battery	May. '96	6	2 → 1
			[2] -19	TCADZ1050YCZZ			Explanation card			1 → 0
			[2] -7	TCADZ1051YCZZ			Supplemental card			
				SSAKAQ014YDE0			Vinyl bag			2 → 1

3. Changes to the parts of the ZR-5000/5700/5800

3-1.Model Name: ZR-5700, ZR-5800, ZR-5800FX

3-2.General: Parts of these units have been changed for the following reasons.

1) In order to prevent the generation of a low noise when the AC adapter is used, the capacitors used at locations C2 and C41 are being changed from ceramic to tantalum.
   When ceramic capacitors were being used at locations C2 and C41, insulation tape was taped on top of them, and a crystal oscillator was bent onto them and attached with glue.
   The tantalum capacitor we have changed to prevent noise generation is about 0.8 mm higher than the old one. As a result we have changed to a crystal oscillator with longer leads. Furthermore, the use of insulation tape has been discontinued.

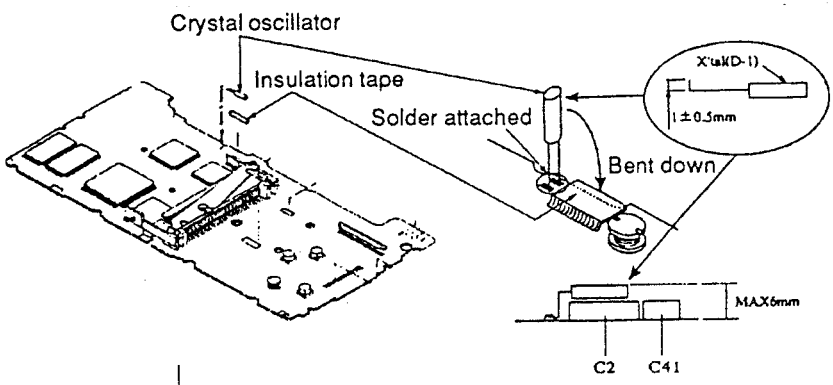


Figure 1:
Diagram for attaching capacitors C2 and C41

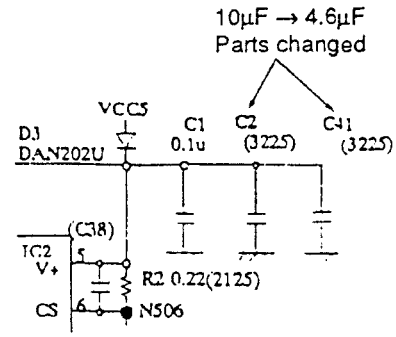
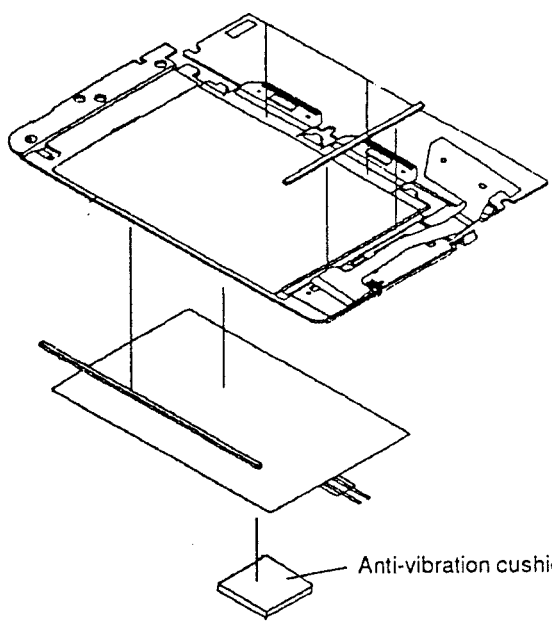


Figure 2:
Circuit diagram for the changed parts

2) In order to prevent the generation of a low noise when the EL backlight is on, an anti-vibration cushion is being added to the EL panel.



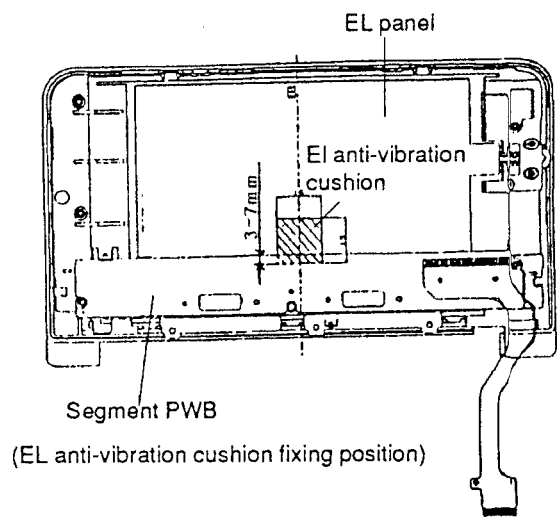


Figure 3:
Diagram for attaching the EL anti vibration cushion

3) In order to comply with CE mark regulations, the key deco film shape has been changed. The operation manual has also been changed slightly due to the addition of a new CE mark statement.

4) The dummy card for the ZR-5000/5700/5800 now includes several languages and is intended for use in all markets.

3-3.Parts Changes:

Ref. No.	Model name	Version	P/G No.	Current parts	New parts		Parts name	Effec-tive time	Inter-change-ability	Note
				Parts code	Parts code	Price rank				
3-1	ZR-5700 ZR-5800 ZR-5800FX	U.S.A. Canada	[4] -36	RCRSP1003PCZZ	RCRSP1007YCZZ	AE	Crystal	Apr. '96	3	
			[1] -75	PTPEH1050PCZZ	—	—	Insulate sheet for crystal		6	1 → 0
			[4] -19	RC-CZ1067RC1C	RC-SZ4751RC1C	AE	Tantalium capacitor [C2, 41]	Mar. '96	3	7 → 5 0 → 2
3-2	ZR-5800	All	[1]	—	PCUSS1014YCZZ	AB	EL noise suppressor sheet	Apr. '96	6	0 → 1
3-3	ZR-5700	All Except U.S.A.	[1] -15	PSHEZ1001YCA3	PSHEZ1001YCA5	AN	Key deco film	May. '96	4	
	ZR-5800			PSHEZ1001YCA4	PSHEZ1001YCA6					
	ZR-5700 ZR-5800		[2] -1	TINSE1049YCZZ	TINSE1049YC01	AS	Operation manual			
3-4	ZR-5000 ZR-5000G ZR-5000I	All	[1] -10	GITA-1001YCZZ	GITA-1001YCZ1	AE	Dummy card	Jun. '96	1	

<Interchange>

1. Interchangeable.	4. Not interchangeable.
2. Current type can be used in place of new type. New type cannot be used in place of current type.	5. Interchangeable if replaced with same types of related parts in use.
3. Current type cannot be used in place of new type. New type can be used in place of current type.	6. Others.

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

[redacted]
ZR-5800-II

SHARP

COPYRIGHT © 1996 BY SHARP CORPORATION
All rights reserved.
Printed in Japan.
No part of this publication may be reproduced,
stored in a retrieval system, or transmitted,
in any form or by any means,
electronic, mechanical, photocopying, recording, or otherwise,
without prior written permission of the publisher.

SHARP CORPORATION
Information Systems Group
Quality & Reliability Control Center
Yamatokoriyama, Nara 639-1 1, Japan
1996 April Printed in Japan Ⓢ